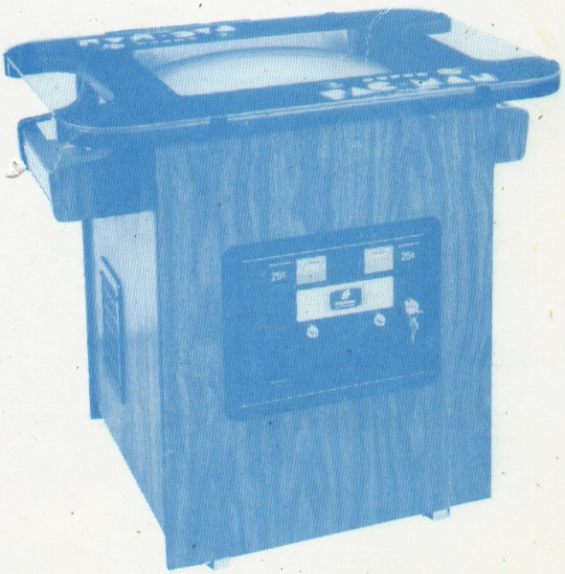
MAY - 4 1983

April, 1983
Game Nos. 316 & 317

Bally/Midway's

SUPER PAC-MAN™

General Information and Troubleshooting Procedures



Bally MIDWAY MFG. CO.

PHONE:
(312) 451-9200
TELEX 72-1596

10601 WEST BELMONT AVENUE
FRANKLIN PARK, ILLINOIS 60131
U.S.A.

PHONE:
TOLL FREE
800-323-7182

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CAUTION: TO PREVENT ELECTRIC SHOCK DO NOT USE THIS (POLARIZED) PLUG WITH AN EXTENSION CORD, RECEPTACLE OR OTHER OUTLET UNLESS THE BLADES CAN BE FULLY INSERTED TO PREVENT BLADE EXPOSURE.

ATTENTION: POUR PREVENIR CHOCS ELECTRIQUES NE PAS UTILISER CETTE FICHE POLARISEE AVEC UN PROLONGATEUR. UNE PRISE DE COURANT OU UNE AUTRE SORTIE DE COURANT, SAUF SI LES LAMES PEUVENT ETRE INSEREES A FOND SANS EN LAISSER AUCUNE PARTIE A DECOUVERT.

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TABLE OF CONTENTS

	Page No.
INTRODUCTION	1
OPTION SWITCH SETTING	5
GAME OPERATION	7
TROUBLE SHOOTING	15
CONTROL INPUTS & OPTION SWITCHES	19
SYSTEM TIMING	23
CPU BOARD BUS STRUCTURE	25
AUDIO CIRCUITRY	29
VIDEO BOARD BUS STRUCTURE	32
VIDEO RAM CIRCUITS	35
COLOR RAM	38
POWER CHASSIS & POWER SUPPLY	40
WIRING DIAGRAM	43
POWER CHASSIS DIAGRAM	44
POWER SUPPLY SCHEMATIC	45
CPU BOARD SCHEMATIC	46
VIDEO BOARD SCHEMATIC	47
SERVICE BULLETINS	48
FUNCTION CHART	BACK COVER

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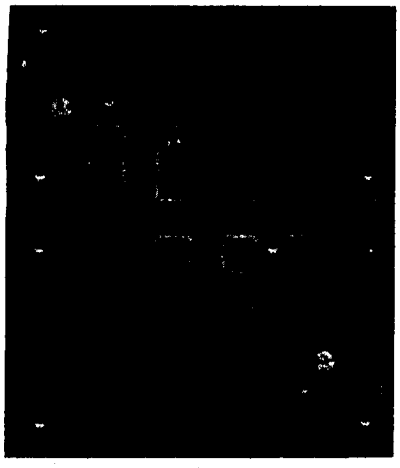
Bally/Midway's

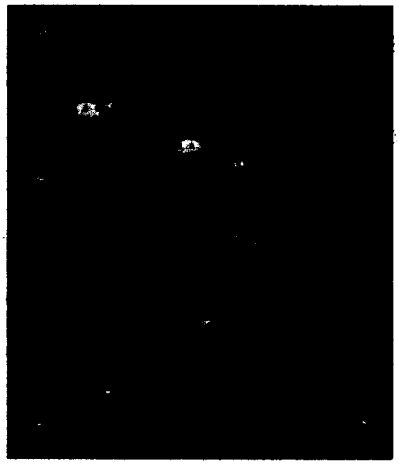
SUPER PAC-MAN™

Bally/MIDWAY T.M.



Conquer the Fruit-Filled Maze!
Play Super Pac-Man and find a super new Pac-Man challenge. Super Pac-Man mazes are made up of delectable fruits and goodies rather than white dots, and also contain 4 energy dots, giving Pac-Man the power to chomp down pursuing monsters, and 2 "Super" dots. When Pac-Man eats a "Super" dot he becomes... SUPER PAC-MAN! Now 10 times his normal size, Super Pac-Man is totally invincible to monsters and can crash through locked gates as he chomps down rows of fruits!

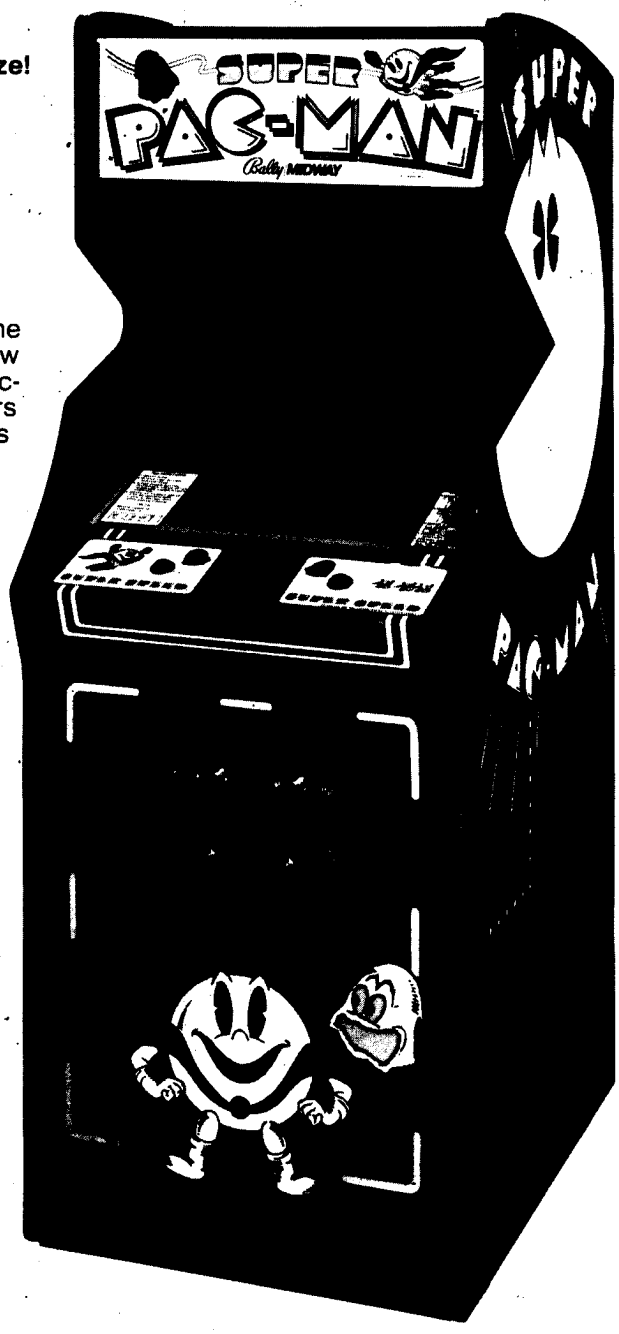
Munch the Keys to Locked Gates!
Each maze contains several locked gates that must be opened before Pac-Man, in regular Pac-form, can pass through. By eating the corresponding keys our hero is free to pass through the gates and devour the fruits or objects inside.



Rack Up Big Bonus Points!
Every third Super Pac-Man maze is a bonus rack. Pac-Man is in "Super" form throughout, racing the clock for Super Pac-Man scores!

At random intervals, a star will flash. When Pac-Man eats the flashing star, he scores bonus points for special fruit/object combinations and matches!

Super Speed for Super Pac-Man
Press Super Pac-Man's super speed button on each side of the joystick and away he goes with an extra burst of speed. Once you push the Super Button you'll be a Super Pac-Man lover forever!



Bally®

MIDWAY MFG. CO.

Cabinet Specifications:

Upright	Mini	Cocktail
Height 73"	Height 60 3/16"	Height 29"
Width 26 1/2"	Width 19 1/2"	Width 32"
Depth 34"	Depth 23 7/8"	Depth 22"

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Franklin Park, Illinois 60131
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Super Pac-Man

IMPORTANT NOTE

DO NOT plug in your new game yet. Before you do anything to your game, we recommend that you read SECTIONS I and II of this manual completely. It will not take more than a few minutes and it may be very helpful.

I. Introduction

SUPER PAC-MAN is a one or a two player game. There are two models: the "UPRIGHT" and "COCKTAL TABLE". When the two player mode is selected on the Upright model, the players take turns at the controls to guide their player through the game course. If you have purchased the Cocktail Table model of this game, the rules of play are the same. The only **difference** is that in the two player mode of the Cocktail Table game, the picture flips to face you when it's your turn.

When playing this game, you are in complete control of SUPER PAC-MAN. He will go wherever you tell him to. And he just loves to eat all the different maze objects (APPLES, BANANAS, DOUGHNUTS, HAMBURGERS, etc.). However, he doesn't like the four ghosts, BLINKY (red), PINKY (pink), INKY (tur quoise), and CLYDE (amber) because they feel the same way about him as he does about the maze objects.

BLINKY, PINKY, INKY, and CLYDE are four **VERY SMART** ghosts. They move very fast and seem to have a sixth sense which always lets them know exactly where SUPER PAC-MAN is in the maze. They never give up in their pursuit of him. One of their favorite tricks is to divide and try to trap him between them. You really have to keep an eye on them.

But SUPER PAC-MAN can turn the tables on these four ghosts for short periods of time during each maze. All he has to do is let them get fairly close in their pursuit of him and then eat one of the POWER DOTS that every maze has in it. When this happens, it causes the four ghosts to turn blue with fright no matter where they are in the maze. This is because they know that when he eats a POWER DOT it gives SUPER PAC-MAN the ability to eliminate them. However, he can **ONLY** eliminate them for as long as they are blue.

The ghosts will only stay blue for a few seconds after SUPER PAC-MAN eats a POWER DOT. But they do give a warning **BEFORE** they turn back to their original colors — they start to flash.

As your skill level increases, the four ghosts speed up their pursuit of SUPER PAC-MAN and they stay blue for **shorter and shorter** periods of time after he eats a POWER DOT until, in the VERY high number mazes, they do not turn blue at all.

Bonus players (this is switch selectable) can be awarded to you as you reach or pass certain preselected point values. The assigned point values for all items that can be eaten are as listed in Figure 1-1.

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Major Features

A major new feature of your SUPER PAC-MAN game is that there are two SUPER POWER DOTS in each maze that, when eaten, will cause your PAC-MAN to turn into a SUPER PAC-MAN. SUPER PAC-MAN can go anywhere within the maze and eat anything that can be eaten. Nothing can stop him.

Game Objective

The object of the game is to **HAVE FUN** and survive as long as possible while constantly improving your skills, eating as many maze objects as you can, and eliminating as many ghosts as possible. As you do this, each following maze will be harder and harder to complete.

OBJECT EATEN	POINT VALUE
APPLES	10 POINTS EACH
BANANAS	20 POINTS EACH
DOUGHNUTS	30 POINTS EACH
HAMBURGERS	40 POINTS EACH
? ? ? ? ?	VARIABLE 50 TO 160 POINTS EACH
KEYS	50 POINTS EACH
POWER DOTS	100 POINTS EACH
SUPER POWER DOTS	200 POINTS EACH
1ST GHOST	200 POINTS
2ND GHOST	400 POINTS
3RD GHOST	800 POINTS
4TH GHOST	1600 POINTS

Figure 1-1 Assigned Point Values

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Super Pac-Man

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INSTALLATION

1. Location requirements:

☐ **Power:**
Domestic 110 V @ 60 Hz
Foreign 200 V to 240 V @ 50 Hz

☐ **Temperature:** 32° to 100° F (0° to 38° C)

☐ **Humidity:** Not over 95% relative

☐ **Space required:**
Upright 25" x 33" (63 x 84cm)
Cocktail 32" x 22" (81 x 55cm)

☐ **Game height:**
Upright 68" (170cm)
Cocktail 29" (73cm)

2. Voltage Selection:

Your game is designed to work properly on the line voltage where you are located. Check your line voltage with a meter to determine what its value is. Then check the power input wires to the main power supply transformer on your game to be sure they are connected to taps which correspond to your line voltage value.

If the power input wires to the main power supply transformer are not connected to taps which correspond to your local line voltage, move them to the proper taps.

If the line voltage in your area falls outside the upper or lower limits of the range of inputs covered by the main power supply transformer, **DO NOT PLUG YOUR GAME IN** until you have talked with your distributor and/or service man and obtained a solution to this problem. Otherwise you could damage your game.

3. Interlock and power ON/OFF switches: See Figure 2-1.

☐ To help prevent the possibility of getting an electric shock while working inside the game cabinet, interlock switches have been installed at each cabinet access door (this **DOES NOT** include the coin door in the Upright models).

☐ When any access door is opened, the interlock switch installed there turns off all power to the game.

☐ Check each interlock switch for proper operation.
After checking the line voltage in your area and determining that the input wires to the main power supply transformer of your game are connected properly — or — after obtaining a solution to your over or under voltage problem from your distributor and/or your service man, plug the game into your A.C. wall outlet.
The game ON/OFF switches for both models are located as shown in Figure 2-1. Turn the game on and allow it to warm up a few minutes.

Slowly open each access door to the game (this **does not** include the coin door on the Upright models).

As the door is opened approximately 1" (2.54cm) the power to the game should go off (the T.V. monitor, all the lights, and all sounds will stop).

If this does not happen, check the interlock switch by this door to see if it has broken loose from its mounting or if it is stuck in the "ON" position.

If the switch is found to be bad, turn the game off, unplug it, and replace the interlock switch.

When done, plug the game back into the wall outlet, close the access door, and turn the game back on.

After the game has warmed up, repeat the above interlock switch test.

When the interlock switch is working properly and turns the power to the game off, power may be restored to the game with the access door(s) open. Take hold of the interlock switch plunger and **gently** pull it out to its fully extended position. THIS IS TO BE USED **ONLY** FOR SERVICING THE GAME. See Figure 2-2.

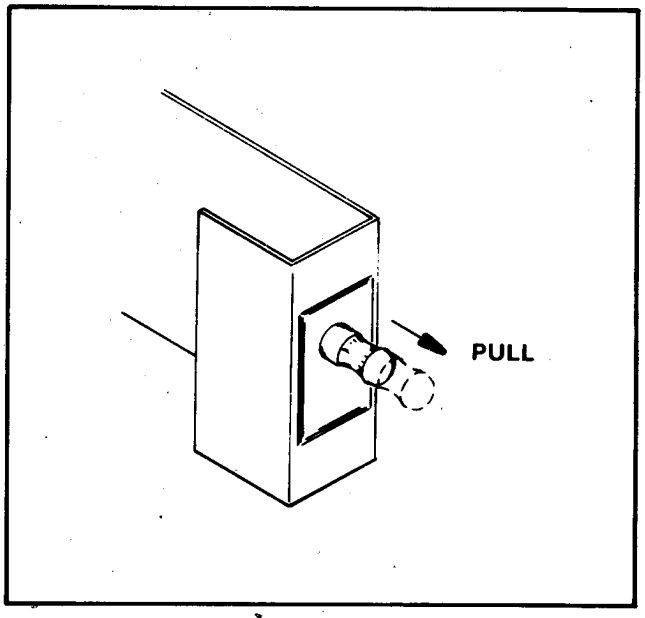

Figure 2-2 Interlock Switch Operation

SELF-TEST

Your new game will Self-Test itself to see if it has any bad parts. The information it receives while testing itself will be shown on the T.V. monitor. Some information can also be heard through the game's speaker system. See the GAME OPERATION section for a more detailed description of this function.

When there is a bad result according to the Self-Test, call your distributor and/or service man to have the trouble fixed unless it is something you can do yourself (such as replace a bad RAM or ROM chip).

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GAME VOLUME ADJUSTMENT CONTROL

See Figure 2-3.

The game volume control pot is located on the game CPU board assembly. There is only one pot. For adjustment, it may be reached through the rear access door on the Upright models. On the Cocktail Table models, you will have to open the table top to reach it.

To make the sounds louder, turn the pot in a clockwise direction ( ).

To make the sounds **less** loud, turn the pot in a counterclockwise direction ( ).

OPTION SWITCH SETTINGS

To change the option switch settings, you DO NOT have to take the Main Game CPU Board out of the game. They can be easily reached through the rear access door on the Upright models. On the Cocktail Table model, you do have to open the table top to reach them.

When changing any options, ALWAYS put the game into the Self-Test mode, make your changes, check the results on the monitor screen, take the game out of the Self-Test mode, and play the game to be sure the switches have worked properly and that no switches were accidentally moved that were not meant to be. (These switches are small and this can happen.)

The option switch settings and what they will make the game do are shown in Figure 2-4. See Figure 2-3 for option switch locations.

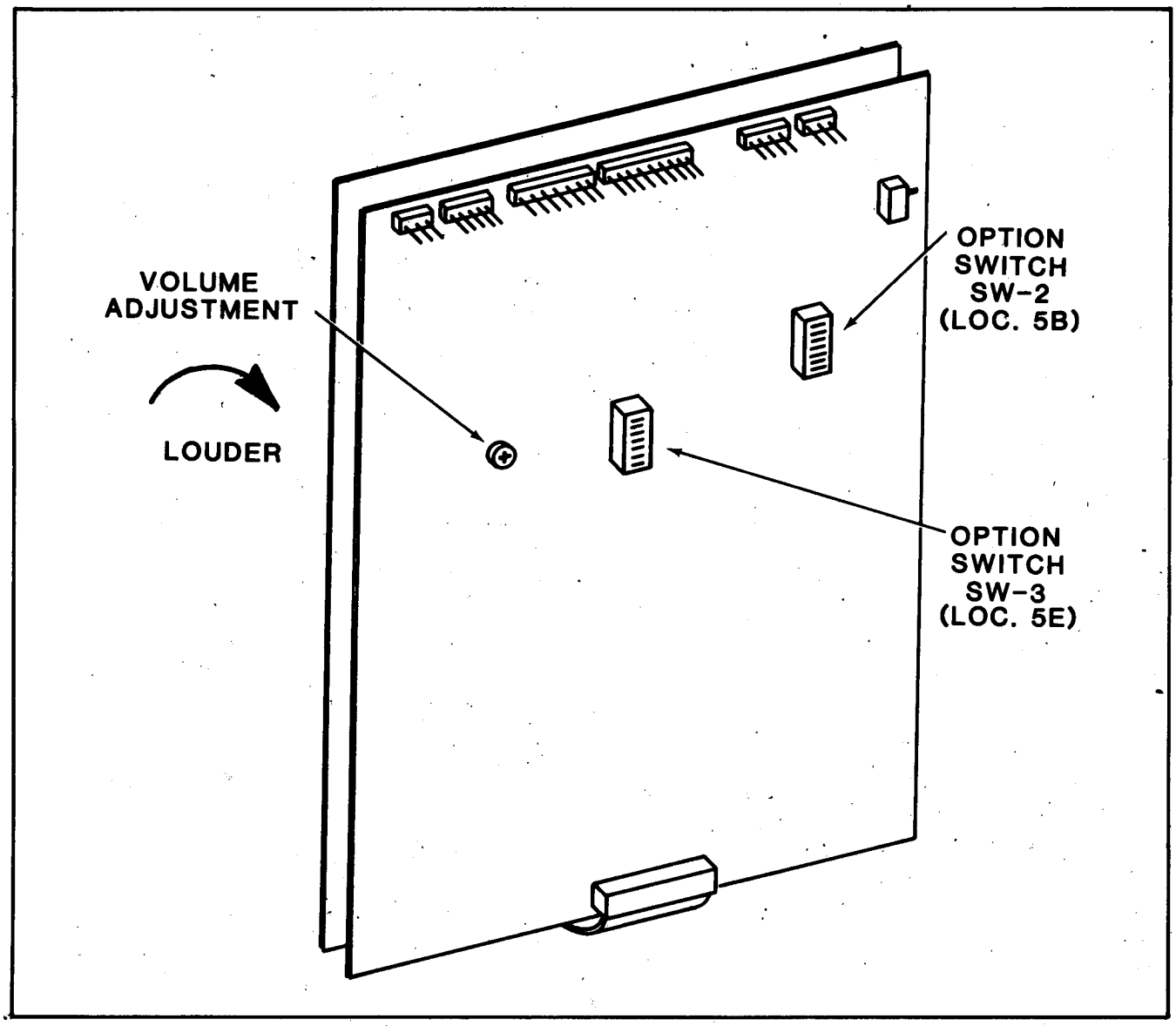

Figure 2-3 Game Volume Adjustment Control & Option Switch Location

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SUPER PAC-MAN

OPTION SWITCH SETTINGS

DIP SWITCH SW-2 AT LOCATION 5B

DIFFICULTY LEVEL SETTINGS — "R1" IS THE EASIEST AND "RB" IS THE MOST DIFFICULT

	SW#1	SW#2	SW#3	SW#4	SW#5	SW#6	SW#7	SW#8
RANK "R0"—STANDARD LEVEL OF DIFFICULTY	OFF	OFF	OFF	OFF				
RANK "R1"—EASIEST LEVEL OF DIFFICULTY	ON	OFF	OFF	OFF				
RANK "R2"	OFF	ON	OFF	OFF				
RANK "R3"	ON	ON	OFF	OFF				
RANK "R4"	OFF	OFF	ON	OFF				
RANK "R5"	ON	OFF	ON	OFF				
RANK "R6"—GRADUATED LEVELS OF DIFFICULTY	OFF	ON	ON	OFF				
RANK "R7"	ON	ON	ON	OFF				
*RANK "R8"—FACTORY SETTING	OFF	OFF	OFF	ON				
RANK "R9"	ON	OFF	OFF	ON				
RANK "RA"	OFF	ON	OFF	ON				
RANK "RB"—HARDEST LEVEL OF DIFFICULTY	ON	ON	OFF	ON				
RANK "RC"—EASIEST **AUTO** DIFFICULTY SETTING	OFF	OFF	ON	ON				
RANK "RD"	ON	OFF	ON	ON				
RANK "RE"	OFF	ON	ON	ON				
RANK "RF"—HARDEST **AUTO** DIFFICULTY SETTING	ON	ON	ON	ON				

SOUND

	SW#1	SW#2	SW#3	SW#4	SW#5	SW#6	SW#7	SW#8
*SOUND							OFF	
NO SOUND							ON	

SCREEN

	SW#1	SW#2	SW#3	SW#4	SW#5	SW#6	SW#7	SW#8
*NORMAL OPERATION							OFF	
FREEZE VIDEO							ON	

*INDICATES FACTORY RECOMMENDED SETTINGS

PART NUMBER MO51-00316-C012

Figure 2-4 Option Switch Settings

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SUPER PAC-MAN

OPTION SWITCH SETTINGS

DIP SWITCH SW-3 AT LOCATION 5E

COINS PER CREDIT — COIN SWITCH 1

		SW#1	SW#2	SW#3	SW#4	SW#5	SW#6	SW#7	SW#8
*1 COIN	1 CREDIT	OFF	OFF	OFF					
1 COIN	2 CREDITS	ON	OFF	OFF					
1 COIN	3 CREDITS	OFF	ON	OFF					
1 COIN	6 CREDITS	ON	ON	OFF					
1 COIN	7 CREDITS	OFF	OFF	ON					
2 COINS	1 CREDIT	ON	OFF	ON					
2 COINS	3 CREDITS	OFF	ON	ON					
3 COINS	1 CREDIT	ON	ON	ON					

BONUS SUPER PAC-MEN AWARDED AT THE FOLLOWING POINT VALUES:

BEGAN WITH 1, 2 OR 3 SUPER PAC-MEN		BEGAN WITH 5 SUPER PAC-MEN		SW#1	SW#2	SW#3	SW#4	SW#5	SW#6	SW#7	SW#8
*1st S P-M	30000	1st S P-M	30000								
2nd S P-M	100000	2nd S P-M	100000				OFF	OFF	OFF		
1st S P-M	30000	1st S P-M	30000								
2nd S P-M	80000	2nd S P-M	120000				ON	OFF	OFF		
1st S P-M	30000	1st S P-M	40000								
2nd S P-M	120000	2nd S P-M	120000				OFF	ON	OFF		
1st S P-M	30000	1st S P-M	30000								
AND EVERY	80000	AND EVERY	100000				CN	ON	OFF		
1st S P-M	30000	1st S P-M	40000								
AND EVERY	100000	AND EVERY	120000				OFF	OFF	ON		
1st S P-M	30000	**ONLY**									
AND EVERY	120000	1st S P-MP	100000				ON	OFF	ON		
ONLY		**ONLY**									
1 S P-M AT	30000	1 S P-M AT	40000				OFF	ON	ON		
NO BONUS SHIPS GIVEN WITH THIS SETTING							ON	ON	ON		

DETERMINES NUMBER OF SUPER PAC-MEN PLAYER BEGINS GAME WITH:

	SW#1	SW#2	SW#3	SW#4	SW#5	SW#6	SW#7	SW#8
*3 SUPER PAC-MEN							OFF	OFF
1 SUPER PAC-MAN							ON	OFF
2 SUPER PAC-MEN							OFF	ON
5 SUPER PAC-MEN							ON	ON

*INDICATES FACTORY RECOMMENDED SETTINGS

PART NUMBER MO51-00316-C012

Figure 2-4 Option Switch Settings (cont.)

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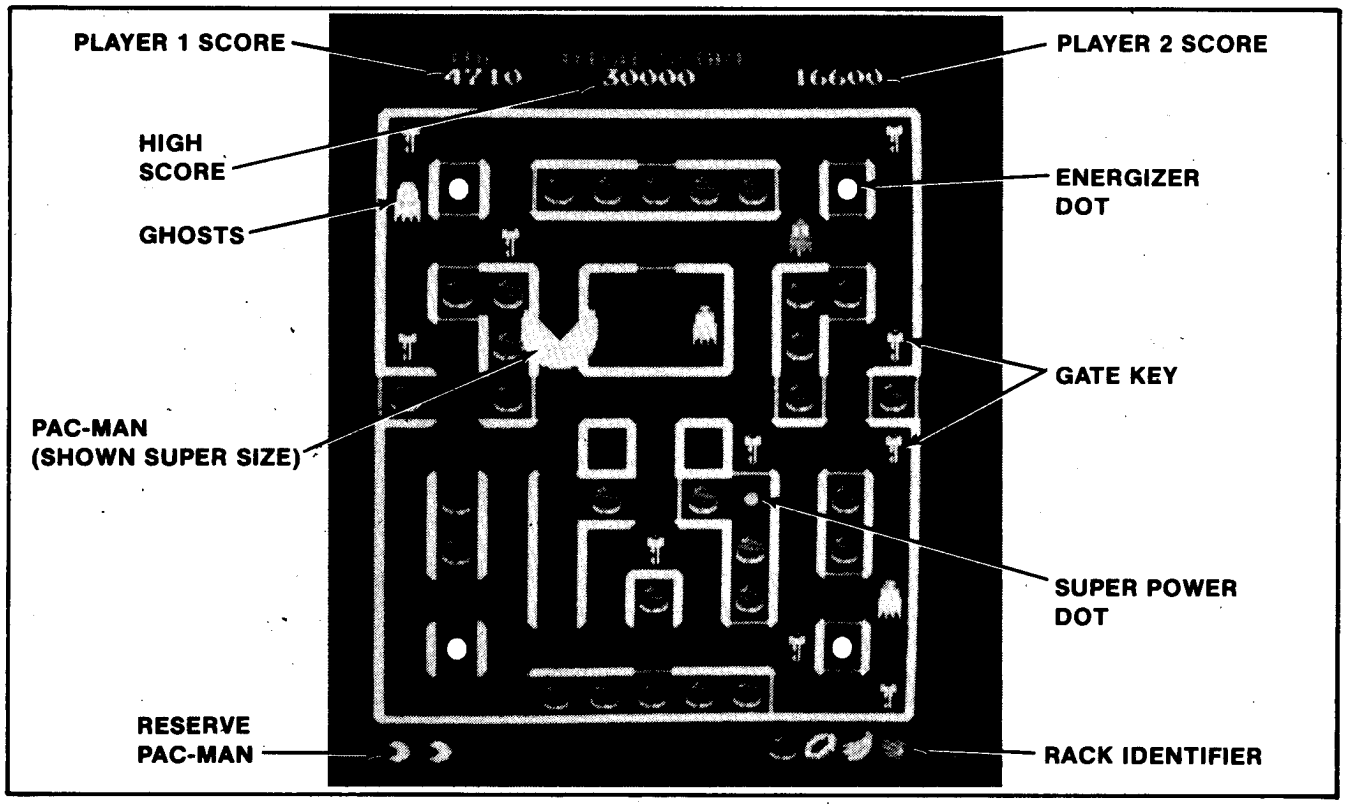
III. Game Operation

SUPER PAC-MAN is a one or a two player game with a color T.V. monitor. The game gives a display which has all the parts shown below.

The game has five possible modes of operation: ATTRACT, READY-TO-PLAY, PLAY, HIGH SCORE/ INITIAL, and SELF-TEST.



Identification of "On Screen" Graphics During Play

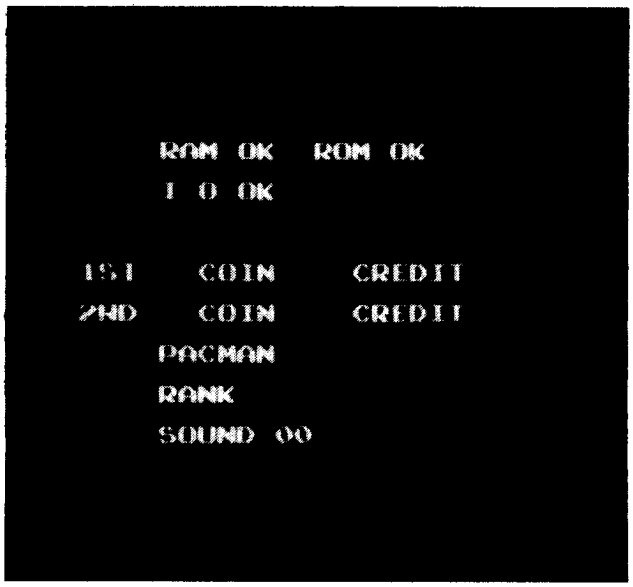
SELF-TEST MODE

The Self-Test mode is a special mode for checking the game switches and computer functions. It is the easiest and best way to check for proper operation of the entire game.

NOTE: Putting the game into Self-Test will cause it to **erase** any CREDITS on the game from its memory.

You may begin a Self-Test at any time by sliding the Self-Test switch to the "ON" position after the power to the game is on. When this is done the game will react as follows:

1. First, you will see random moving multicolored patterns on the screen.
2. Immediately following this, a rightside up test display is shown on the monitor screen. This will remain until you set the Self-Test switch back to the "OFF" position. This test display is shown at right.



Self-Test — Menue

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3. If a bad ROM or RAM chip is found by the game's internal check system during the Self-Test, the game indicates this to you by showing the location code of the bad chip(s) on the SCREEN. The following table translates the chip location codes into the actual position on the game's P.C. Boards.

RAM TEST INDICATIONS AND THEIR MEANINGS

INDICATION	MEANING	CHIP LOCATION
RAM OK	NO RAM IS OUT OF ORDER	
RAM 1	RAM 1 on VIDEO PCB is no good	2E
RAM 2	RAM 2 on VIDEO PCB is no good	2H
RAM 3	RAM 3 on VIDEO PCB is no good	2K
RAM 4	RAM 4 on VIDEO PCB is no good	2J
RAM 5	RAM 5 on C P U PCB is no good	3K
RAM 6	RAM 6 on C P U PCB is no good	3L
RAM 7	RAM 7 on C P U PCB is no good	2D

ROM TEST INDICATIONS AND THEIR MEANINGS

INDICATION	MEANING	CHIP LOCATION
ROM OK	NO ROM IS OUT OF ORDER	
ROM 1	ROM 1 on C P U PCB is no good	1C
ROM 2	ROM 2 on C P U PCB is no good	1B
ROM 3	ROM 3 on C P U PCB is no good	1K

I/O TEST INDICATIONS AND THEIR MEANINGS

INDICATION	MEANING	CHIP LOCATION
I/O OK	NO BIT IS OUT OF ORDER	
I/O 1	BIT C P U 1 is out of order	4F
I/O 2	BIT C P U 2 is out of order	4C

4. To check your game function switches and buttons (coin counter switches, TEST CREDIT button, 1 PLAYER and 2 PLAYER buttons): activate each one while the game is in the Self-Test mode. You should hear a game sound for each activation. If you do not hear it, the switch/button is either not working, miswired, or disconnected. Check it out thoroughly.
5. RANK is a difficulty level setting with "R1" being the easiest and "RB" being the most difficult level of play. "RC" through "RF" are AUTO difficulty level settings with "RC" being the easiest and "RF" the hardest setting. In "AUTO" the game measures the player's skill level and **AUTOMATICALLY** gets harder as his/her skill level improves.
6. When finished with the Self-Test mode, slide the Self-Test switch back to the "OFF" position.

- ☐ A cross hatch pattern appears on the monitor screen for about 2 seconds.
- ☐ If you wish to keep this test pattern on the monitor screen for further use, slide Self-Test switch back to the "ON" position after the cross hatch appears and before it disappears.
- ☐ When finished with the cross hatch pattern, set the Self-Test switch to the "OFF" position.
- ☐ Normal game functions will now return to the monitor screen.

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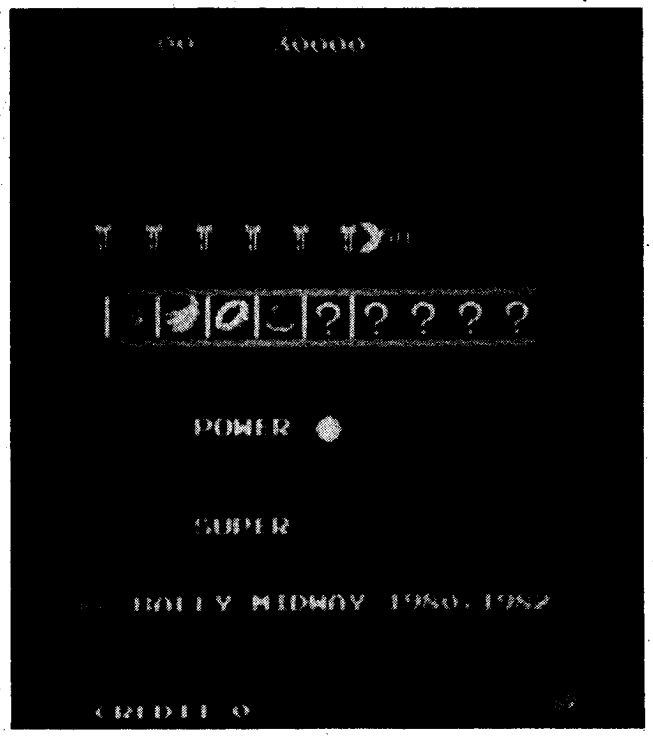
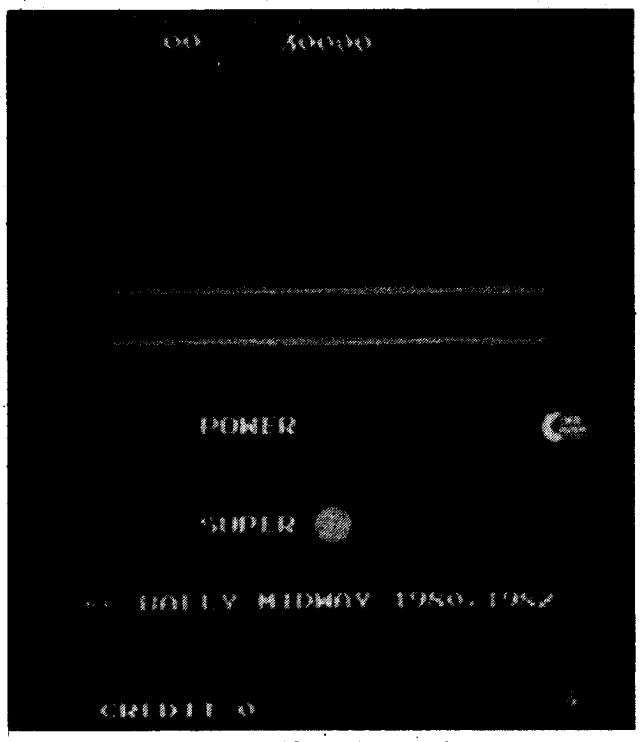
ATTRACT MODE

1. The Attract mode starts:

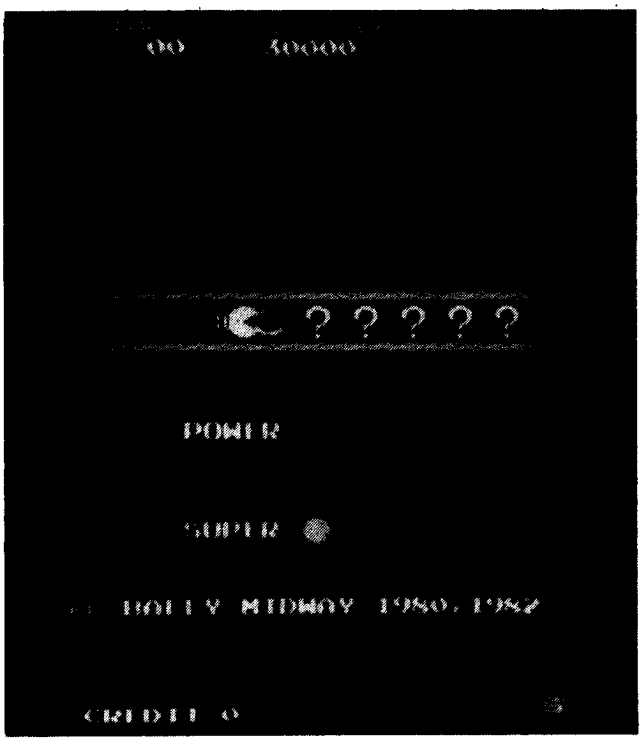
- ☐ Just after power has been turned on to the game. (Self-Test switch is in the "OFF" position.)
- ☐ After a Self-Test has been completed. (Performing a Self-Test sets the credits in the game's memory to zero "0".)
- ☐ After a play has been finished and there are no more credits left in the game's memory.
- ☐ In the Attract mode, the game will give the following displays **centered** on the monitor screen:



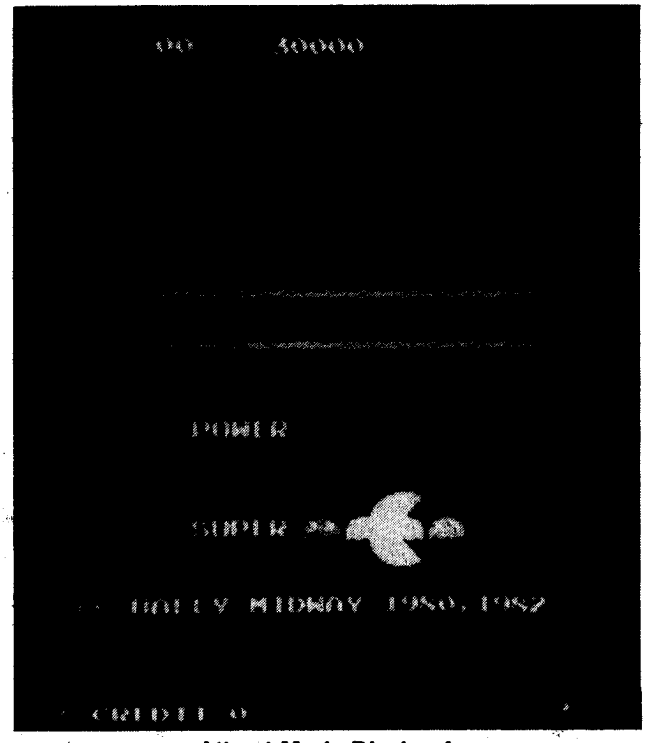
Attract Mode Display 1



Attract Mode Display 3



Attract Mode Display 2



Attract Mode Display 4

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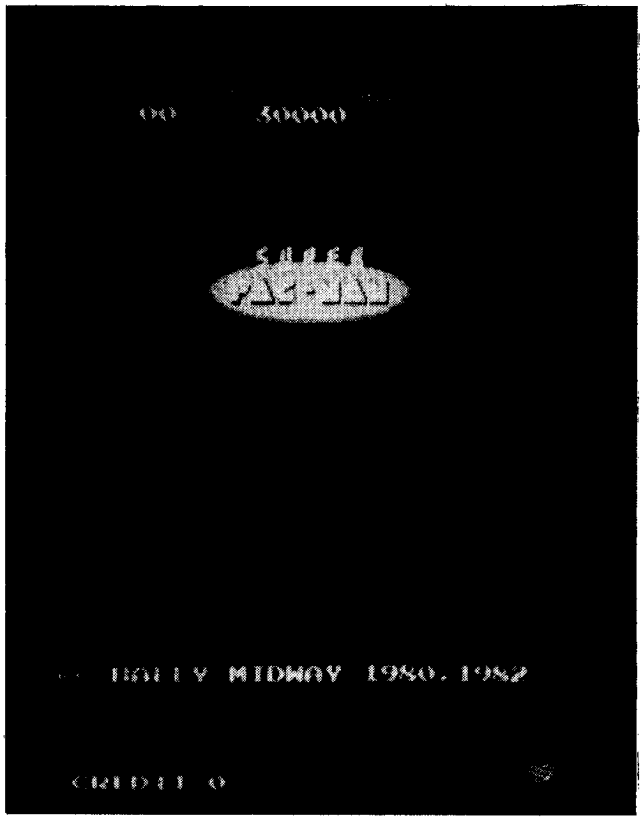
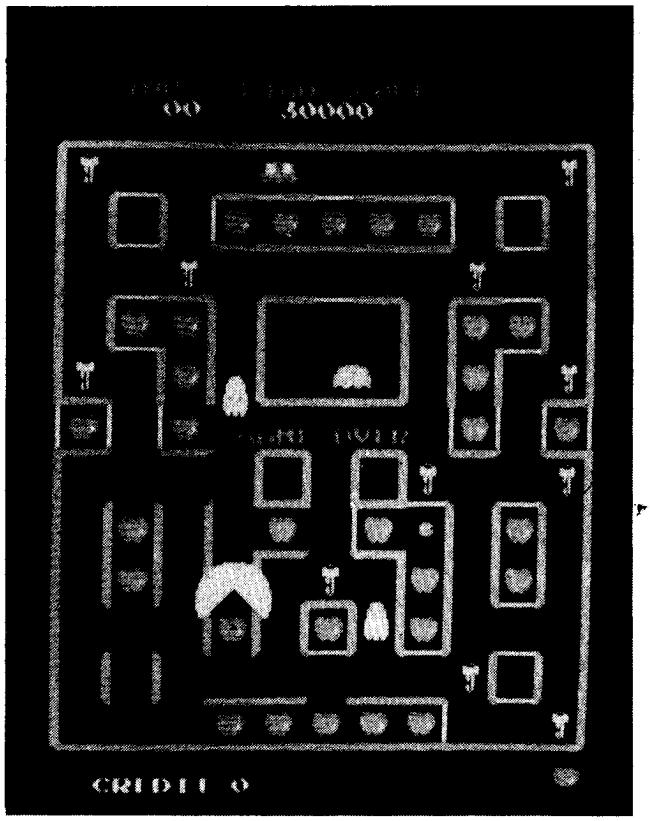
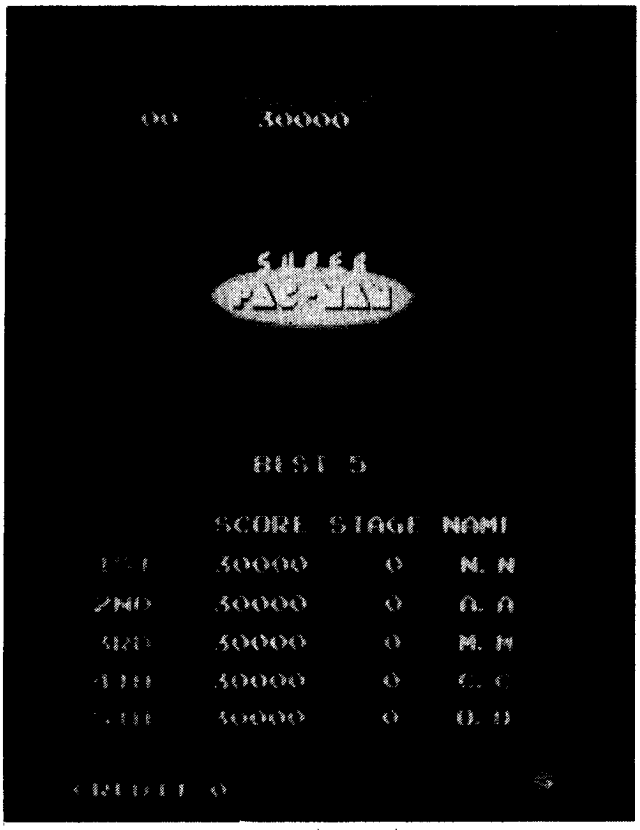


Attract Mode Display 5



Attract Mode Display 7



Attract Mode Display 6

☐ No matter where the game is in the Attract mode sequence, it will immediately go to the following display as soon as a game has been paid for. It will hold this display on the monitor screen until the "1 PLAYER" or "2 PLAYER" start button is pushed.

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Ready to Play Mode Display 1

Ready to Play Mode Display 2

READY-TO-PLAY MODE

1. The Ready-To-Play mode starts when enough coins have been accepted for a 1 or a 2 player game.
2. The Ready-To-Play mode ends when either the "1 PLAYER" or the "2 PLAYER" push button is pressed.
3. In the Ready-To-Play mode, the game will give one of the above displays **centered** on the monitor screen.
4. If no START button is pressed, the game will hold this display on the screen indefinitely.

PLAY MODE

1. The Play mode begins when the "1 PLAYER" or the "2 PLAYER" start button is pressed. "STAGE 1" "10 PTS" is displayed and then "PLAYER ___ READY!" is displayed below the "GHOST HOUSE" on the screen.
2. The Play mode ends when your last SUPER PAC-MAN has been eliminated. When this happens, "PLAYER ___ GAME OVER" is written across the center of the monitor screen (below the "GHOST HOUSE").
3. The game consists of a single maze with side exits. The items that your SUPER PAC-MAN wants to eat are located in maze corridors with locked doors at every possible entrance to them. You must direct your PAC-MAN to eat the KEYS positioned around the maze in order to gain access to these sealed corridors. The only other way he can get at the food he wants to eat is to eat the KEY that opens the door to one of the two SUPER POWER DOTS in each maze and then eat that SUPER POWER DOT.

   When he does this, your PAC-MAN grows to SUPER size and can munch his way through all the locked doors in the maze. YOU can give YOUR Pac-Man SUPER SPEED while he is SUPER size by pressing the SUPER SPEED button on the control panel. He will now move through the maze at a **much faster** pace. However, you will find that he is harder to steer when he is traveling at this SUPER SPEED and you will also notice that he stays SUPER size for a much shorter period of time when traveling at SUPER SPEED.
4. At the beginning of each game, SUPER PAC-MAN appears right below the center of the "GHOST HOUSE" while the four ghosts appear at the "GHOST HOUSE". BLINKY appears outside the doors and PINKY, INKY, and CLYDE appear inside the "GHOST HOUSE".
5. When play begins, BLINKY (who'd love to eliminate him) immediately begins looking for SUPER PAC-MAN (who immediately begins eating KEYS just as fast as he can). As time passes, PINKY, INKY, and CLYDE (who'd also love to eliminate him) leave the "GHOST HOUSE" one at a time and begin looking for SUPER PAC-MAN — who is still busily eating KEYS and maze food just as fast as **YOU** can steer him to them.

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But with all four ghosts chasing him, it is not as easy to eat the KEYS and maze food (without being eliminated by a ghost) as it was earlier in the game. And BLINKY, PINKY, INKY, and CLYDE are four **VERY SMART** ghosts. For instance, they will divide up two, three, or four ways to try to trap SUPER PAC-MAN between them, in a corner, or even in one of the tunnels. You've really got to watch them! It seems like they always have some sneaky new trick up their sheets.

However, if they get too close, SUPER PAC-MAN can always eat one of the flashing POWER DOTS. When this happens, it causes all four ghosts to turn blue with fright no matter where they are in the maze. This is because they know that when he eats a POWER DOT it gives SUPER PAC-MAN the ability to eliminate them. But, he can **ONLY** eliminate them for as long as they are blue. And they will only stay blue for a short period of time. But the ghosts do give a warning **BEFORE** they turn back to their original colors — they start to flash.

When SUPER PAC-MAN eliminates a blue ghost, its point value appears on the monitor screen at the place where the ghost was eliminated while at the same time being added to your score, and the ghost disappears — all except for its eyes. The eyes go back to the "GHOST HOUSE" where they get another body of their original color. This done, they leave the "GHOST HOUSE" again and take up their pursuit of SUPER PAC-MAN once more.

When he eats the last item of any particular maze: all movement stops immediately, the maze flashes and disappears. Next, the game displays "STAGE ___" "___ PTS" and the next maze appears. All the players are in the new maze when it appears. The words "PLAYER ___ READY!" are also there — right below the "GHOST HOUSE". After a second or two passes, the words "PLAYER ___ READY!" disappear and play begins.

You **MUST** eat all the food in any particular maze in order to advance to the next one.

The maze identifier symbols appear at the bottom edge of the monitor screen.

As your skill level increases, the four ghosts speed up their pursuit of your SUPER PAC-MAN and they stay blue for **shorter and shorter** periods of time after he eats a POWER DOT until, in the high number mazes, they do not turn blue at all.

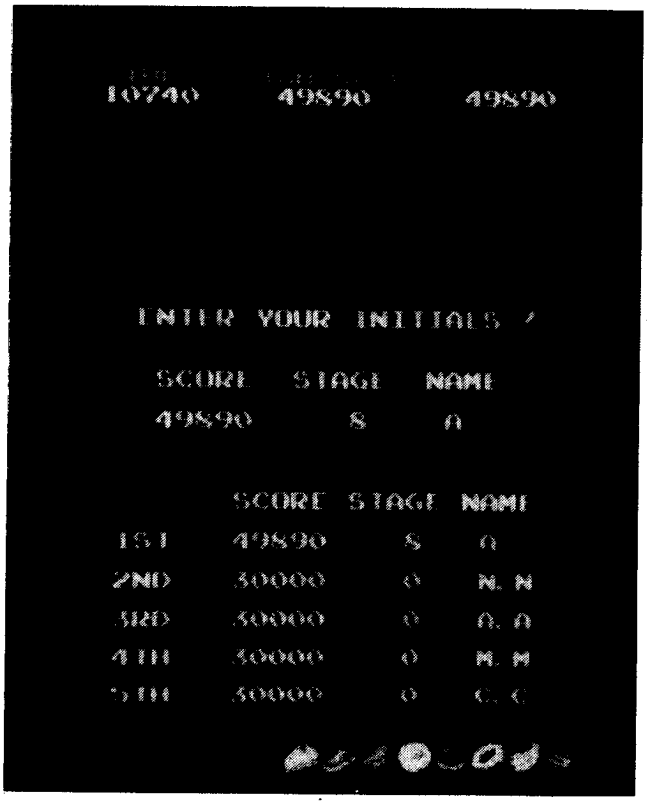
Bonus players (this is switch selectable) can be awarded to you as you reach or pass certain preselected point values. The assigned point values for all items that can be eaten are as listed in Figure 1-1.

When one of the ghosts happen to eliminate one of your SUPER PAC-MEN, assuming you have at least one remaining in reserve, the maze disappears. Next, the game displays "STAGE ___" "___ PTS" and the maze re-appears. All the players are in the new maze when it reappears. The words "PLAYER ___ READY!" are also there — right below the "GHOST HOUSE". After a second or two passes, the words "PLAYER ___ READY!" disappear and play begins anew.

When one of the ghosts eliminates your **LAST** SUPER PAC-MAN, the words "GAME OVER" are displayed below the "GHOST HOUSE", your score is displayed under "1 UP", and in addition, if your score was the highest on this game to date, it will also be displayed under "HIGH SCORE" at the top center of the monitor screen and go into the HIGH SCORE/INITIAL MODE. If your score was **NOT** the highest but was still one of the best five scores to date, the game will then also go into the HIGH SCORE/INITIAL MODE. After this the game will then either go into the Ready-To-Play mode (if there are still credits left in its memory) or into the Attract mode (if there are no more credits left in its memory).

If your score was not high enough to cause the game to go into the HIGH SCORE/INITIAL MODE, it will then either go into the Ready-To-Play mode (if there are still credits left in its memory) or into the Attract mode (if there are no more credits left in its memory).

Most of the above holds true in the "2 PLAYER" mode also. But there are a few minor differences.



High Score/Initial Mode

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TWO PLAYER OPERATION

The Upright and Cocktail Table models both have two player operation.

In the two player mode, the rules of play are the same as in the single player mode. There are some additional rules, however.

1. In the Upright model, the players must take turns at the controls.
2. In the Cocktail Table model, each player has his own set of individual controls. The picture will flip to face you when it is your turn. (When it is not your turn, your set of controls will have **NO** effect on the game.)
3. Your turn lasts until one of the ghosts eliminates your SUPER PAC-MAN. At this point, the game will do one of several things depending on whether or not the eliminated SUPER PAC-MAN was your last or if you still have others remaining in reserve.

SUPER PAC-MAN ELIMINATED — OTHERS REMAINING IN RESERVE

- ☐ The chase stops.
- ☐ Next, the game displays "STAGE ___" "___ PTS", the screen display changes to the screen display of the other player, it displays "PLAYER ___ READY!" under the "GHOST HOUSE" at the same time one of the other player's reserve SUPER PAC-MAN appears.
- ☐ After a second or two passes, the words "PLAYER ___ READY!" disappear and play begins for the other player.

SUPER PAC-MAN ELIMINATED — NO OTHERS REMAINING IN RESERVE

- ☐ Game displays the words "PLAYER ONE" or "PLAYER TWO" "GAME OVER" below the "GHOST HOUSE".
- ☐ Your final score is displayed under "1 UP" or "2 UP", depending upon which player you were. In addition, if your score was the highest on this game to date, it will also be displayed under "HIGH SCORE" at the top center of the monitor screen and go into the HIGH SCORE/INITIAL MODE. If your score was **NOT** the highest but was still one of the best five scores to date, the game will then also go into the HIGH SCORE/INITIAL MODE. After this the game will display "STAGE ___" and "___ PTS". The other player's maze appears along with the words "PLAYER ___ READY!" under the GHOST HOUSE. After a few moments, the words "PLAYER ___ READY!" disappear and play begins for the other player.

  If your score was not high enough to cause the game to go into the HIGH SCORE/INITIAL MODE, it will then display "STAGE ___" and "___ PTS". The other player's maze appears along with the words "PLAYER ___ READY!" under the GHOST HOUSE. After a few moments, the words "PLAYER ___ READY!" disappear and play begins for the other player.
- ☐ After the **last** player's **LAST** SUPER PAC-MAN has been eliminated, if his score was not high enough to cause the game to go into the HIGH SCORE/INITIAL MODE, it will then either go into the Ready-To-Play mode (if there are still credits left in its memory) or into the Attract mode (if there are no more credits left in its memory).

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Troubleshooting

Introduction

The most common problems occur in harness components such as the coin acceptor, player controls, interconnecting wiring, etc. The TV monitor and PCB computer cause their share of problems too, but not as much as the harness and its component parts. TV monitor troubleshooting will not be covered here because it is covered in that section of this manual.

As you already know, the PCB computer is a complex device with a number of different circuits. Some circuits remain basically the same among games, but overall there are a great many differences between them. PCB troubleshooting procedures, therefore, can be lengthy and will differ greatly among games. However, some basic Z-80 CPU information is involved in this section.

General Suggestions

The first step in any troubleshooting procedure is correctly identifying the malfunction's symptoms. This includes not only the circuits or features malfunctioning, but also those still operational. A carefully trained eye will pick up other clues as well. For instance, a game in which the computer functions fail completely just after money was collected may have a quarter shorting the PCB traces. Often, an experienced troubleshooter will be able to spot the cause of the problem even before opening the cabinet.

After all the clues are carefully considered, the possible malfunctioning areas can be narrowed down to one or two good suspects. Those areas can be examined by a process of elimination until the cause of the malfunction is discovered.

Harness Component Troubleshooting

Typical problems falling in this category are coin and credit problems, power problems and failure of individual features.

NO GAME CREDIT

For example, your prospective player inserts his quarter and is not awarded a game. The first item to check is if the quarter is returned. If the quarter is returned, the malfunction most certainly lies in the coin acceptor itself. First, use a set of test coins (both old and new) to ascertain that the player's coin is not undersize or underweight. If your test coins are also returned, coin acceptor servicing is indicated. Generally, the cause of this particular problem is a maladjusted magnet gate. Normally, this will mean slightly closing the magnet gate a little by turning the adjusting screw out a bit (see section on coin acceptor for more details).

If the quarter is not returned and there is no game credit, the cause of the malfunction may be in one of several areas. First try operating the coin return button; if the coin is returned, the problem is most likely in the magnet gate. Enlarge the gap according to the coin acceptor service procedures. If this does not cure the problem, remove the coin acceptor, clean it and perform the major adjustment procedure.

If the trapped coin is not returned when the wiper lever is actuated, you may have an acceptor jammed by a slug, gummed up with beer, a jammed coin chute, or mechanical failure of the acceptor mechanism. In this case, first check for the slug that will generally be trapped against the magnet. If so, simply remove the slug and test the acceptor. If the chute is blocked, remove the acceptor and remove the jammed coins. If there is actual failure of the acceptor, remove the unit and repair as indicated in the coin acceptor service procedures.

If the coin is making its way through the acceptor (that is, falling into the coin box), yet there is still no game credit, you either have a mechanical failure of the coin switch or electrical failure of the coin and credit circuits. The first place to begin is by checking the coin switch. Most of these switches are the make/break variety of micro switch, which is checked by testing for continuity between the NO, NC, and C terminals. When not actuated, the NC and C terminals should be continuous and the NO terminal open. When operated, the NO and C terminals should close and the NC should be open. If the coin switch checks out, examine the connections to the terminals to make sure there is good contact. If necessary, use the continuity tester and check from the terminal lug on the switch to the associated PCB trace. This will tell you if there is a continuous line all the way to the credit circuit.

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If the coin switch wires do not check out, the problem is in the computer — most likely in the coin and credit circuitry.

If you do get game credit when a coin is deposited, but the game will not start when the start switch is pressed, you may have a problem in the start switch, the interconnecting wiring or in the computer. First check the switch. If the switch is OK, proceed to check the wiring. Again, make sure you go from the terminal lug on the switch to the PCB trace. This way, you will check the terminal contact as well as PCB edge connector contact. If the wiring is continuous, proceed to check the PCB credit circuit. If not, check each section of the wiring, until the discontinuity is located. If the wiring is OK, the problem must lie in the computer.

Transformer and Line Voltage Problems

Your machine must have the correct line voltage to operate properly. If the line voltage drops too low, a circuit in the computer will disable game credit. The point at which the computer will fail to work will vary some from game to game, but no game will work on line voltage that drops below 105 VAC.

Low line voltage may have many causes. Line voltage normally fluctuates a certain amount during the day as the total usage varies. Peak usage times occur mainly at dawn or dusk, so if your machine's malfunction seems to be related to the time of day, this may be a factor. A large load connected to the same line as the game (such as a large air conditioner or other device with an exceptionally large motor) may drop the line voltage significantly when starting up. This drop can result in an intermittent credit problem. In addition, poor connections in the location wiring, plug, or line cord may also cause a significant drop in power. Cold solder joints in the game's harness, especially in areas like the transformer connections, interlock switch, or fuse block, may also produce the same results, although probably on a more permanent basis.

Sometimes location owners (especially in bars) replace light switches with dimmer rheostats, and the game is sometimes on the same line. Obviously, the voltage available to the game is going to drop dramatically when the dimmer is turned.

In any case, the way to check for correct line voltage is with your VOM. Set the VOM to 250 VAC and stick the probes in the wall receptacle. If it's OK here, check the transformer primary connections. If you do not get 117 VAC, examine the solder joints on the transformer, fuse block, and interlock switch. If you do get 117 VAC, the problem must be either in the transformer, harness connections, or in the PCB power supply.

If you suspect the transformer, check its secondaries with the VOM set to 50 VAC and correlate the readings with the legend on the side of the transformer. The transformer must also be correctly grounded, so check the ground potential as well, especially if there is a hum bar rolling up or down the TV screen.

HARNESS PROBLEMS

Other harness problems include blowing fuses and malfunctioning controls. The repeating blown-fuse problem can sometimes be quite exasperating to solve, for short circuits have the tendency to occur in areas almost impossible to find. First, try inserting a new fuse, as old fuses age and blow without cause. If the new one also blows, you definitely have a short.

The best way to approach this problem is by turning the power off and disconnecting devices that may be causing the problem, such as the TV, transformer, and PCB. Disconnect the devices by pulling off their connectors, but do not allow them to touch. If necessary, insulate them with small pieces of electrical tape. Then, connect your VOM across the terminals of the fuse block (all electrical power shut off), and set it to one of the resistance scales. This will save blowing a fuse each time you want to check the circuit.

If the VOM reveals that disconnecting the devices removed the short, reconnect the devices one by one until the short returns. The last device connected is the one that is at fault. If the VOM reads a short even after the devices are disconnected, the fault must lie in the harness itself, and only patient exploration will reveal its location. First, carefully examine all the wiring, looking for terminals that may be touching, metal objects such as coins shorting connections or burned insulation. If necessary, use the VOM to check each suspected wire.

MALFUNCTIONING CONTROLS

One of the most common problems here is a bad potentiometer. Typically, a bad pot will cause the image to jump as it reaches a certain point. The only cure for this one is to install a new pot.

If a feature that is operated by a switch (for example, joysticks, foot pedals, control panel buttons) does not operate at all, check the switch with a VOM or continuity tester to verify its operation. If the switch does not check out, replace it. If the switch is OK, you should suspect the input to the switch from the PCB. In this case, get out the harness and logic schematics and check to see what kind of input it is. In many cases, the input will be +5 VDC. If so, use the VOM to check its presence. Normally, the switch is used to pull a +5 VDC line LOW to GND or to pull a LOW line HIGH. If the PCB output is missing, check the wire length from the PCB. If you find the signal at the PCB trace, the wire length or connection is at fault. If not, begin exploring the PCB using the logic schematics.

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CONTROL INPUTS AND OPTION SWITCHES

As in all Midway games the player controls use normally open switches with one pole of each switch connected to common or logic ground. The other pole of each switch is connected to the input circuits on the CPU board via the wiring harness.

Examine the PLYR1-LEFT (player one move left) input on J2-2. Pin number 2 of connector J2 will normally read +5 volts. When the player one joystick is moved left pin number 2 of J2 should drop to 0 volts. If it does not drop to 0 volts there is a problem in the switch or wiring. If J2-2 responds correctly but the Pac-Man will not move left, the problem is on the CPU board.

Following the PLYR1-LEFT line the first component is a .01MF capacitor, C77. This capacitor is connected between the PLYR1-LEFT line and earth ground to filter out any noise or static discharge that might enter the line. If C77 is missing or broken, the circuit will still operate but the line will lack static protection. If this capacitor is shorted the PLYR1-LEFT line will read 0 volts and the Pac-Man will move left automatically.

The 1K ohm resistor in package RM15 pulls the line up to +5 volts. If this resistor is missing or broken the line will read 0 volts.

The 2.2K ohm resistor in package RM14 is used to protect the 56XX custom input component at location 4F. If this resistor is broken or missing, pin number 25 of the 56XX will read 0 volts and the Pac-Man will move left automatically.

Capacitor C21 is used to debounce the PLYR1-LEFT control line. When a control switch is first closed its contacts bounce and might send a series of pulses to the 56XX at 4F. A capacitor connected between the control line and logic ground will discharge upon switch closure and reduce the bouncing to a single smooth pulse. If the debounce capacitor is broken or missing the circuit will operate but the 56XX will see numerous pulses for a single switch closure. A missing debounce capacitor on line J2-7 or J2-8 could mean numerous credits for a single coin. If the debounce capacitor is shorted, pin 25 of the 56XX will read 0 volts and the Pac-Man will move left automatically.

After discussing the RRCC network on the PLYR1-LEFT line one can see that if the line reads 0 volts the Pac-Man will move left automatically (unless the 56XX is faulty). If the line reads correctly up to pin 25 of 4F but the Pac-Man does not respond properly, the 56XX is probably faulty.

It is not always noticeable when there is a bent pin or missing signal at the 56XX. If pins 1 and 3 are removed from the circuit the game will appear to function normally. In most cases however a bent pin or missing signal to 4F will cause the game to be stuck in self test and the symptom "I/O-1" will appear on the second line of the test.

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Another 56XX custom input chip is located at position 4C. This second device receives data from the DIP SW packages SW2 and SW3 at positions 5B and 5E. Note that data from SW3 is multiplexed thru the 74LS157 at 4E before reaching the 56XX.

Multiplexing allows the eight lines of data from SW3 to share only four lines between 4E and the 56XX. There are eight inputs on a 74LS157 (four "A" inputs and four "B" inputs) and four outputs (1Y, 2Y, 3Y and 4Y). When the select line on pin 1 is low, data on the "A" inputs will appear on the "Y" outputs. When the select line is high, the "B" inputs will appear on the "Y" outputs. In this manner either input 1A or 1B can be transferred to output 1Y depending on which input the 56XX needs to examine. The strobe line on pin 15 of 4E must be low for the 74LS157 to operate.

The eight lines of data from SW2 are pulled-up to +5 volts thru 4.7K ohm resistors in resistor package RM1. When a switch in SW2 is OFF, the corresponding input on the 56XX will read +5 volts. When the switch is ON, the input will read 0 volts. If the pull-up resistor on a SW2 line is faulty or missing the line will read 0 volts and the 56XX will not recognize when that switch is off.

Data from the self test switch enters the CPU board on J2-14 and data determining whether the board is used as an upright or table model comes in on J2-15. When J2-15 is high the board responds as an upright game. When J2-15 is low the board will respond as a table model and flip the picture upside down for the second player. In an upright cabinet J2-15 is not used so the line reads +5 volts because of the pull-up resistor R20. In a table cabinet an extra wire in the harness connects J2-15 to common or logic ground so the line reads 0 volts.

Both lines J2-14 and J2-15 are conditioned by RRCC networks before reaching the 56XX. A faulty RRCC component on either line will cause the line to read 0 volts.

The 2H*, 4 reset and $\overline{\text{VBLANK}}$ signals feed pins 1, 2 and 4 of both 56XX components. The eight output pins (9, 10, 11, 12, 34, 35, 36, 37) on both 4C and 4F are also connected in parallel. Note that outputs 9, 10, 11 and 12 feed a 74LS157 multiplexer at position 3E while outputs 12, 34, 35, 36 and 37 feed the 16XX custom bus controller at position 4B. A faulty signal, bent pin or broken trace on any of these eight output lines will cause the game to be stuck in self test and to display "I/O-1". Also if the signals on pins 5 and 6 of either 4C or 4F are missing the game will be stuck in self test.

Switches 1, 2 and 3 of SW3 at location 5E determine pricing. Switches 4, 5 and 6 of SW3 determine the scores required to earn bonus Super Pac-Men. Note that the score required to earn the bonus will differ depending on whether the game is set to start with 1, 2 or 3 Super Pac-Men or 5 Super Pac-Men. Switches 7 and 8 of SW3 set the number of Super Pac-Men the game will start with.

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SW2 at location 5B is used to set the difficulty level of game play. There are twelve fixed levels of difficulty and four automatic difficulty levels. Switch 7 of SW2 determines whether or not the game sounds will occur during the attract mode. Switch 8 is very useful for diagnosing the game. When switch 8 is turned ON the game play will freeze. The picture and sound will remain frozen as long as switch 8 is ON.

A "rack test" is also available using switch 8 of SW2. To enter the "rack test" coin and start a game. Then just as the Super Pac-Man begins to move, turn switch 8 ON. Now each time the FAST (or speed) button is pushed the next maze in the game sequence will appear on the screen. Using this "rack test" option one can obtain any maze in the sequence without playing the game.

Data concerning the status of the player controls and option switches (SW2 and SW3) leaves the 16XX custom bus controller from pins 7, 8, 10, 11, 12 and 13. This data is then either stored in the 2114 RAM at 2D or passed thru the 74LS245 at 2E to the buffered main data bus. If any of these six outputs are missing or incorrect the game may be stuck in self test displaying "RAM 7" or "I/O-1". So a "RAM 7" display in self test does not necessarily mean that the RAM at 2D is bad. As one can see a faulty 16XX or bad D10 thru D14 line could be the problem. An incorrect signal on pins 1, 3, 4, 5 and 6 of the 16XX will also cause the game to be stuck in self test displaying "RAM 7" or "I/O-1".

Outputs 9, 10, 11 and 12 of both 56XX components become the "B" inputs to a 74LS157 multiplexer at position 3E. The "Y" outputs of multiplexer 3E are used as address lines (A6, A7, A8 and A9) to the 2114 RAM at 2D. When the select line to 3E is low, BMA0 thru BMA3 from the buffered main address bus appear at the address lines to RAM 2D. When the select line is high, outputs 9, 10, 11 and 12 of the 56XX components are used to address RAM 2D.

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SYSTEM TIMING

System timing starts with the 18.432MHz crystal and the 74LS368 inverting buffer at position 4A. The signal from pin 11 of 4A is used to clock both flip-flops at position 3B. The 2Q output from pin 10 of 3B is inverted to become the 6MB, 6MSYNC and 6M (6 megahertz) signals. The 6M signal is ORED with the 1H signal thru the 74LS32 at position 3C. Pin 8 of 3C is used to clock the flip-flop at 2A. Pin 9 of flip-flop 2A yields the Q signal which is used at pin 35 of microprocessor 1A and pin 34 of microprocessor 1L.

In the Pac-Man and Ms. Pac-Man systems a chain of binary counters are used to divide the 6 megahertz signal to produce the H & V timing signals. In Super Pac-Man this is accomplished by two 07XX custom components at positions 1N on the CPU board and 2C on the video board.

The 07XX at position 1N on the CPU board outputs the equivalents of the H timing signals from pins 2 thru 8. The 07XX on the video board outputs the equivalents of the V timing signals.

Starting with the 1H signal from pin 2 of the 07XX on the CPU board each pin up to pin 8 is 1/2 the frequency of the preceding pin. The 1H signal is 3MHz. The 2H signal is 1.5MHz and pin 4 (4H or A20) is 1/2 that frequency or .75MHz etc.

The H timing signals are necessary to synchronize the microprocessor circuits. 2H is inverted and then used at pin 34 of microprocessor 1A. The 2H* signal from pin 11 of buffer 2H is used at pin 35 of microprocessor 1L. The outputs of the 07XX are also used to address RAMS 3K and 3L and to control the 15XX custom component in the audio circuitry.

The outputs of the 07XX on the video board are processed thru an 00XX custom address generator at position 2D. The outputs of the 00XX are used to address RAM 2E and are gated thru 1F, 1B and decoder 1C. Pins 12, 13, 14 and 15 of decorder 1C are used as $\overline{EG}$ (tri-state control) inputs to the bus transceivers at 1E, 1H, 1J and 1K. Pins 3, 6, 8 and 11 of chip 1B are the CS signals to RAMS 2E, 2H, 2J and 2K. Addressing to RAMS 2H, 2J and 2K also requires the outputs from the 00XX. MA17 thru MA20 are outputs from gates 1F and MA30 thru MA36 are outputs from the 04XX custom address generator. Note the timing signals controlling gates 1F and the 04XX.

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BUS STRUCTURE
(CPU BOARD)

Microprocessor 1A is master to microprocessor 1L. Both microprocessors are supported by their own PAL, ROM and bus control circuitry. Timing on pins 34 and 35 of 1A and 1L synchronizes the operation of both microprocessors. Besides interfacing with their related circuits some communication must occur between the microprocessors themselves.

The MAIN address bus from microprocessor 1A services the program ROMS, PAL 2B and decoder 2C and is then buffered thru 74LS367 components at positions 1E, 1H and 2H to become the buffered MAIN address bus (BMA0 thru BMA15).

The SOUND address bus (SA0 thru SA15) from microprocessor 1L services the SOUND ROMS and PAL 1M. SA0 thru SA9 supply the A inputs to multiplexers 3F, 3H and 3J. Note that the B inputs to the multiplexers are supplied by BMA0 thru BMA9 from the MAIN address bus. The outputs of the multiplexers will coincide with either the BMA bus or the SOUND address bus depending on the condition of the 1H signal or the outputs will be held in tri-state by the 2H signal.

The 2H signal on pin 15 of the multiplexers controls the Y outputs. When the 2H signal is low the A or B inputs will appear at RAMS 3K and 3L. When the 2H signal is high the Y outputs are disabled to allow a third source of addressing to the RAMS. The 07XX at position 1N and the 15XX at position 3N provide the third address bus. Pins 4, 5, 6, 7 and 8 of the 07XX and pin 6 of the 15XX supply address lines A20 and A25 after being buffered thru a 74LS367 at position 2N.

The 1H signal on pin 1 of the multiplexers is used to select the A inputs or the B inputs to appear on the Y outputs. When the 1H signal is high the BMA bus will service RAMS 3K and 3L. When the 1H signal is low the SOUND address bus will service the RAMS.

The 1H signal is twice as fast as the 2H signal so while the 2H signal is low the 1H signal will have time to select the A inputs and the B inputs and both microprocessors will have a chance to address RAMS 3K and 3L. While the 2H signal is high the multiplexer outputs are disabled and addressing from the 07XX and the 15XX will service the RAMS. Note that address lines A20 thru A23 are decoded by a 74LS259 at position 2M to provide the reset and interrupt signals for the two microprocessor circuits and that the buffered MAIN address bus is sent thru a ribbon cable to the video board.

The eight data lines on pins 24 thru 31 of the 68A09E microprocessor are bidirectional. Data can flow into or out of the microprocessor on these eight lines. Of course data can only move along these lines in one direction at a time. Only one signal can have access to a data line at any moment in time.

The 68A09E at position 1A can read from program ROM 1B or 1C (1D is not used) when the 2H* signal on pin 22 of the ROMS is low and the R/$\overline{W}$ signal at pin 6 of the 74LS138 at 2C is high.

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When the R/$\overline{W}$ signal from pin 32 of microprocessor 1A is high the decoder at position 2C will decode the MA13, MA14 and MA15 address lines. Depending on the status of these address lines one of the decoder outputs will be driven low while the other decoder outputs remain high.

If decoder output Y6 or Y7 is driven low the corresponding ROM will have access to the MAIN data bus. The decoder at 2C assures that only one program ROM can have access to the data bus at any moment in time.

The MAIN data bus from microprocessor 1A is buffered thru a bidirectional bus transceiver at position 1F. The direction that data passes thru the 74LS245 is controlled by the R/$\overline{W}$ signal on pin number 1. Note that this R/$\overline{W}$ signal is from pin 19 of the PAL at 2B and should not be confused with the R/$\overline{W}$ signal from pin 32 of microprocessor 1A. The 74LS245 can be disabled by a high signal on pin 19 to isolate the MAIN data bus from the buffered MAIN data bus (BMD0 thru BMD7). When the MAIN data bus and the BMD bus are isolated microprocessor 1A can communicate with the program ROMS and the BMD bus is free to interface with RAMS 3K, 3L and 3D and the buffered SOUND data bus.

The SOUND data bus from microprocessor 1L services SOUND ROM 1K and is buffered thru a 74LS245 at position 2K to interface with RAMS 3K, 3L and the 15XX at 3N. The direction data passes thru 2K is controlled by the R/$\overline{W}$ signal from pin 32 of microprocessor 1L. The SOUND 2 signal controlling the E$\overline{G}$ pin on 2K comes from PAL 1M.

After the bidirectional bus transceiver at 2K, the buffered SOUND data bus (BSD0 thru BSD7) is tied directly to RAMS 3K, 3L and the 15XX. The BSD bus can communicate with the buffered MAIN data bus thru the 74LS245 at position 2F.

It is the bidirectional bus transceiver at 2F that allows the two microprocessors to communicate with one another. Chip 2F also allows both microprocessors to have access to RAMS 3K, 3L and 2D.

Bus transceivers 1F and 2F are both controlled by the R/$\overline{W}$ signal from PAL 2B so both will pass data in the same direction (A inputs to B inputs or B inputs to A inputs) at the same time. The E$\overline{G}$ (bus isolation control) signal to chip 1F comes from PAL 2B pin 12 but the E$\overline{G}$ to chip 2F is the SOUND signal from pin 18 of PAL 2B so both transceivers will not necessarily be enabled at the same time.

Note another bidirectional bus transceiver at position 2E. Again the direction of data flow thru 2E will be the same as thru chips 1F and 2F because pin 1 of 2E is controlled by the R/$\overline{W}$ signal from PAL 2B. The FBIT signal from PAL 2B controls the E$\overline{G}$ input of bus transceiver 2E.

Suppose that bus transceivers 1F, 2F and 2E are enabled by low signals on the E$\overline{G}$ inputs and

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that the R/$\overline{W}$ signal from PAL 2B is high. Data can now pass from the A inputs to the B inputs of each bus transceiver. Data from RAM 2D could now pass thru chips 2E and 1F to microprocessor 1A or data from the 16XX in the control input circuits could reach microprocessor 1A. If bus transceiver 2E is disabled the buffered SOUND data bus can pass thru chips 2F and 1F to microprocessor 1A and RAMS 3K and 3L can be read by microprocessor 1A.

Now suppose the R/$\overline{W}$ signal from PAL 2B is low so that data can pass from the B inputs to the A inputs of the bus transceivers. The MAIN data bus could now pass thru chips 1F and 2E to RAM 2D or thru chips 1F and 2F to either RAMS 3K and 3L or to the 74LS245 at position 2K and microprocessor 1L.

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AUDIO CIRCUITRY

The microprocessor at 1L, ROM 1K and the PAL at 1M are dedicated to the audio circuitry. Timing and control signals for the 68A09E microprocessor at 1L are not the same signals used for the microprocessor at position 1A. The Q signal from the clocking circuit is buffered thru 2H for the E timing input on pin 34 and the 2H* signal from pin 11 of buffer 2H is used as the Q timing input on pin 35. The $\overline{\text{RESET}}$ input on pin 37 of this microprocessor uses the SUBRESET signal from pin 10 of the 74LS259 at position 2M. The $\overline{\text{IRQ}}$ input on pin 3 is once again the $\overline{\text{Q}}$ output of a flip-flop at 2J but here the flip-flop is cleared by the INTON2 signal from pin 4 of the 74LS259 at 2M.

The PAL at 1M controls the CS (chip select) and OE (output enable) on ROM 1K. SRAMWR (sound RAM write) is gated thru the 74LS08 at 4J to control R/W to RAMS 3K and 3L.

LTWR (latch write) is connected to pin 14 of the 74LS259 (8 bit addressable latch) at position 2M to enable this latch. Note that the INTON2 and SUBRESET signals which are critical for operation of the microprocessor at 1L are outputs of this latch. At the same time, the microprocessor 1L and the PAL at 1M must be operating properly to generate the LTWR signal which enables the latch. So we see a loop between the microprocessor circuit in the audio system and the 74LS259 latch at position 2M. Also the LATCH and SNDWR (sound write) signals controlling the PAL at 1M are outputs of the PAL at 2B in the main microprocessor circuit. The sound system microprocessor is subordinate to the main microprocessor circuitry. So a failure at PAL 2B or in the main microprocessor circuits can disrupt the entire audio system.

Data from ROM 1K can be bused directly to microprocessor 1L. To communicate with the RAMS at 3K and 3L the sound data bus must pass thru a 74LS245 at position 2K. The bidirectional bus transceiver at 2K is enabled by the SOUND 2 signal from PAL 1M. Microprocessor 1L delivers a R/$\overline{\text{W}}$ signal to pin 1 of 2K. This R/$\overline{\text{W}}$ signal determines which direction data can pass thru the 74LS245.

Although the schematic shows a 64K ROM at 1K and a 32K ROM at 1J only position 1K is used. If the 32K ROM used at 1K is faulty the game will be stuck in self test with the display ROM 3. If the 2148 RAM at 3K is missing or faulty the game will display RAM 5 and if RAM 3L is faulty the game will display RAM 6.

Data on the A side of 2K is referred to as the "buffered sound data bus" (BSD0 thru BSD7). Besides communicating with RAMS 3K and 3L the BSD bus controls the 15XX custom address generator at position 3N. The 15XX might be considered the first component in the circuit that actually generates the game sounds.

The 15XX uses some of the H timing signals, the BSD bus and 18.432MHz from the clock circuit to generate addressing for the PROM at position 3M. If pins 1, 2, 3 or 5 of the 15XX are not

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receiving the correct signal the self test will read O.K. but there will be either no sound or just hissing and clicking thru the speaker. If pin 4 does not receive the correct signal the game will be stuck in self test displaying RAM 5. If pins 6, 7 or 8 do not output the correct signal or if these signals do not reach their destinations the self test will read O.K. but there will be no sound in the game mode. It has been found that if a BSD line is removed from the 15XX or if the outputs from the 15XX do not reach the PROM at 3M the game sounds will be present but distorted. Usually a missing BSD line or output from the 15XX will cause the game sounds to be faster or higher in frequency.

The 4 bit nibble from pins 9, 10, 11 and 12 of PROM 3M is the data to be modified and then presented to the final audio amplifier at position 5N. This nibble supplies the 5D, 6D, 7D and 8D inputs to the octal flip-flops at 4M and will appear on the 5Q, 6Q, 7Q and 8Q outputs when the SOUND ON signal is high. After 4M, each of the four lines are assigned a value of resistance. Note that starting with resistor R34 each resistor up to R37 is 1/2 the value of the preceding resistor. R35 is 1/2 the value of R34. R36 is 1/2 the value of R35 and R37 is 1/2 the value of R36. After this "resistor ladder" all four lines are shorted together. This circuit is commonly referred to as an "analog adding circuit".

Because all four lines are tied together after the analog adding circuit we now have a single line of data. This single line of data can be passed thru any of the four electronic switches in package 4L. Examine the bottom switch in the 4066 (quad bilateral switch package) at 4L. Data from the analog adder circuit can enter pin 1 and exit pin 2 whenever pin 13 is high. If the control pin 13 is low the switch is open and data will not pass thru. The control signals on pins 13, 6, 5 and 12 of the 4066 are supplied by BSD0 thru BSD3 at the 1Q, 2Q, 3Q and 4Q outputs of 4M.

After the bilateral switches we find another analog adding circuit (R22, R23, R24 and R25). Again the four lines are tied together to form a single line of audio data. The line is pulled-up to +5 volts by resistor R27 and held from logic ground by resistor R17 and capacitor C25. If capacitor C25 is shorted the line will be pulled-down to 0 volts causing loss of all game sounds. Resistor R26 and VR1 (volume control) can cause loss of all sounds if they are missing or faulty.

The MB3730 at position 5N amplifies the audio signal and sends two active lines to the speaker. The MB3730 requires approximately +12 volts on pin 7. This +12 volts is only used for the audio circuit so the game will operate properly without it except for the absence of the game sounds.

An easy way to check the MB3730 for amplification is to turn the volume control up all the way and then to tap a finger on pin number 1. If the tapping can be heard thru the speaker the MB3730 is amplifying.

Pins 5 and 6 are the outputs of the MB3730. If capacitors C27, C28 or C84, C85, C86 and C87 are faulty, sound or volume will be lost.

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BUS STRUCTURE
(Video Board)

The tri-state buffered MAIN address bus (BMA0 thru BMA15) from microprocessor 1A on the CPU board enters the video board thru connector P1 and the ribbon cable. The 07XX custom component at position 2C on the video board generates vertical timing signals which are sent to the 00XX at 2D. The outputs from the 00XX are tri-state and tie in with the BMA signals so that either the BMA bus or the vertical timing signals can address RAM 2E. When the FLIP signal on pin 27 of the 07XX is high the picture will flip upside down for the second player in a table model game. The FLIP signal is derived from the BMD0 signal by a 74LS74 flip-flop at position 4A on the video board.

The combined BMA/vertical timing bus is also required by the 04XX custom component at position 2F, the 74LS138 decoder at 1C and the 74LS32 OR gates at position 1F.

The outputs from decoder 1C and ANDED thru a 74LS08 at 1B to provide the chip select signals for RAMS 2H, 2J and 2K. MA30 thru MA36 from the 04XX provide the low order addresses to RAMS 2H, 2J and 2K while MA17 thru MA20 from the OR gates at 1F provide the high order addresses. Note the numerous signals required by the 04XX.

The buffered MAIN data bus (BMD0 thru BMD7) also enters the video board thru connector P1 and the ribbon cable. The BMD bus is buffered thru bidirectional bus transceivers 1E, 1H, 1J and 1K to provide four separate data buses on the video board.

Data bus "A" (D50 thru D57) from bus transceiver 1E services the 2K X 8 RAM at 2E and the octal flip-flop packages at 1D and 4F. The outputs from flip-flops 1D and 4F are used to address ROMS in the final video stages.

Data bus "1" (D10 thru D17) from bus transceiver 1K services RAM 2K and the 12XX custom component at position 3J. The 12XX is used to address the 8K X 8 character ROM at position 3F. Data bus "1" is also used as the preset inputs to binary counters 1M, 2M, 1N and 2N which address the video RAMS 4M and 4N.

Data bus "2" (D20 thru D27) services RAM 2J and the 12XX custom component.

Data bus "3" (D30 thru D37) services RAM 2H and the 12XX custom component. D30 thru D35 is latched thru a 74LS378 at position 3K to address a ROM at 3L. D32 thru D37 is latched thru a 74LS273 at position 3H to provide addresses A8 thru A12 and "chip select" for character ROM 3F.

Each of the data buses ("A", "1", "2" and "3") on the video board has access to a 2K X 8 RAM (RAMS 2E, 2H, 2J and 2K). Each of the four data buses and their associated RAMS are used to address character ROMS 3C or 3F.

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Data bus "A" is latched thru octal flip-flops at 1D to address character ROM 3C. Note that addresses A0 thru A3 of ROM 3C are supplied by the 1V, 2V, 4V and 4H signals on the inputs of XOR gates at 3B. When the FLIP signal on the XOR gate inputs is low, the V and H signals will pass thru unchanged. When the FLIP signal is high, the H and V signals will be inverted by the XOR gates. The XOR gates at 3B are being used as part-time inverters to flip the picture for the second player in table model games.

The character ROM at 3C generates the maze image. If it is removed from the circuit the blue maze lines and the pink gates will disappear from the picture. The game will play normally without ROM 3C and the characters will respond as if the maze is present but the maze will be invisible. The 8 bit bus from 3C is loaded into the 11XX custom component at position 3D to be converted to serial form and then passed to the final video circuits.

The 12XX custom component at position 3J receives data from buses "1", "2" and "3" and converts it to addresses A30 thru A35 which supply the A0, A1, A2, A5, A6 and A7 inputs of character ROM 3F. The 2764 ROM shown at position 3E on the schematic is not used in Super Pac-Man.

D32 thru D36 from data bus "3" is latched thru a 74LS273 at position 3H to supply the A8 thru A12 address inputs of ROM 3F. Output pins 8 and 11 of the XOR gates at 4H supply the A3 and A4 inputs to character ROM 3F. Note that the FLIP signal is used to control the 4H* and 8H* signals thru the XOR gates so that address inputs A3 and A4 will be inverted when the picture is flipped. The $\overline{2H}$ signal controls the OE (output enable) of ROM 3F and the CS (chip select) input is supplied by the D40 signal from pin 12 of the 74LS273 at 3H.

Character ROM 3F generates the moving characters and the keys. If ROM 3F is removed from the circuit the game will play normally but Super Pac-Man, the ghosts and the keys will be square blocks instead of defined images. The square blocks are referred to as the "window" or "hit zone" for each character.

The 8 bit data buses from character ROMS 3C and 3F are loaded into the 11XX custom component at position 3D. The 11XX converts the sixteen data lines from the character ROMS to four lines of serial data. Pins 11 and 12 of the 11XX provide addresses A0 and A1 for the ROM at 4E while pins 17 and 18 provide A0 and A1 to the ROM at 3L. The signal from pin 3 of NAND gate 4B, the signal from pin 3 of XOR gate 4H and the FLIP signal control the 11XX custom component.

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VIDEO RAM CIRCUITS

The D2148 RAMS (1K X 4) at 4M and 4N store the images of Super Pac-Man, the ghosts and the various fruits and maze symbols while they're being shifted around the screen. If either video RAM is faulty the characters may have thin lines thru their bodies, their eyes may be the wrong size and color, tiny dots might appear on the screen or thin lines might run from top to bottom across the entire screen. The characters might be duplicated many times or shifted to the wrong position on the screen if these RAMS are faulty. As one can see, a bad video RAM can cause numerous problems with the graphics but the game will still coin and play thru the program.

To determine which video RAM is faulty use a wire connected to +5 volts and momentarily force the RAM outputs high one at a time and observe the screen. IMPORTANT: If the output of an integrated circuit is forced high or low for too long a period of time, the component may be damaged. Cutting the RAM output pins will cause the same response as forcing them high without causing the RAM to burn out.

In a good circuit each video RAM output will cause a change in some of the characters when it is forced high or cut. In a faulty circuit, check each video RAM output to find the output that either does nothing or eliminates the symptom when it is forced high.

Data bus "1" from bus transceiver 1K is used to preset the binary counters at positions 1M, 2M, 1N and 2N. Data on the A, B, C and D inputs of a 74LS161 binary counter will be transferred to the QA, QB, QC and QD outputs whenever the L (load) input is low. Data from bus "1" is loaded into the binary counts to set a starting address to video RAMS 4M and 4N when the $\overline{\text{HSET}}$ signal from pin 13 of buffers 3M and 3N forces the L inputs low. When the L inputs are high, the counters will increment the address to RAMS 4M and 4N by one count for each pulse on the CK inputs of the counters. Note that the CK inputs are driven by the 6M signal from pin 11 of the 74LS368 at position 2B on the video board.

If an address line to the video RAMS is faulty thin vertical lines may appear thru the characters and keys or their images may be duplicated many times on the picture. An easy way to isolate the faulty address line is to momentarily force each address line low with a jumper wire connected to logic ground (0 volts). The faulty address line will usually cause no change on the picture when it is forced low.

Data bus "3" from bus transceiver 1H is latched thru a 74LS373 at position 3K to provide D50 thru D55 which address a ROM at 3L. The four bit nibble from ROM 3L is buffered thru chip 3M to tie in with the outputs of RAM 4M and thru chip 3N to the outputs of RAM 4N. Note that each of the outputs from buffers 3M and 3N is pulled up to +5 volts thru either resistor pack RM1 or RM2.

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The four bit nibble from ROM 3L is also NANDED thru a 74LS20 at position 4J. Pin 6 of NAND gate 4J is then NANDED with the OBJEN (object enable) and $\overline{6M}$ signals to supply the 1A and 4B inputs to multiplexer 4K. The 6MB and $\overline{HSYNC}$ signals also supply inputs to multiplexer 4K. The outputs of chip 4K are used as WE (write enable) to RAMS 4M and 4N and as CL (clear) to the binary counters.

The four bits of data (DD10 thru DD13) from ROM 3L and RAM 4N provides word 2 to the 74LS298 at position 4L. DD20 thru DD23 from ROM 3L and RAM 4M provides word 1 to the 74LS298. The 74LS298 is a quad 2 to 1 line multiplexer with storage capabilities. When the 1V signal on pin 10 is low, word 1 will appear on the QA thru QD outputs. When the 1V signal is high, word 2 will be transferred to the Q outputs. The four bit word from multiplexer 4L is then sent to a custom PAL at position 4D.

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THE COLOR ROM

The five output lines from PAL 4D are used to address a 32 X 8 ROM at position 4C. This color ROM determines the color and color intensity for each point on the monitor screen. As the monitor scans a given point on the screen the color ROM will output an eight bit word to turn on various combinations of the red, green and blue guns in the picture tube. Note that the eight outputs are arranged in three groups. D0, D1 and D2 provide the red signal; D3, D4 and D5 provide the green signal; D6 and D7 provide the blue signal for the monitor. Note also the resistor ladder or analog adder circuit for each of the three groups of outputs from the color ROM. The resistor ladder offers more or less resistance to the color signal resulting in a more or less intense color on the screen.

Examine the D0, D1 and D2 output lines from the color ROM. If D2 is high while D0 and D1 are low, the color signal will pass thru R5 (220 ohms) to produce an intense red point. If D0 is high while D1 and D2 are low, the color signal will have to pass thru R3 (1K ohms) which is more than four times the resistance of R5 (220 ohms) resulting in a much dimmer red point. Of course a point of medium intensity red would occur if D1 is high while D0 and D2 are low.

All the colors a monitor is capable of producing are derived from the primary colors red, green and blue. To obtain the color purple for example, the color ROM would output the byte 10000100 to turn on the blue and red guns simultaneously. Since white is a mixture of equal parts of red, green and blue, the byte 11110110 is used to create a white point on the screen. Note that the "byte for white" uses the 220 ohm and 470 ohm paths for each of the three primary colors. This can be verified by putting the game into the cross hatch mode and checking the outputs of the color ROM. During the cross hatch mode pins 2, 3, 5, 6, 7 and 9 are active, while pins 1 and 4 remain low.

The color ROM 4C may cause blurry shadows behind the characters or complete loss of video if it is faulty. If either of the 100pf capacitors on the outputs of the three color signals is shorted that color will be lost. Usually if the alphanumerics in the self test are white one can be sure that the color ROM and the color outputs are functioning properly because all three primary colors are necessary to produce a white spot on the screen.

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THE POWER CHASSIS AND POWER SUPPLY BOARD

The power chassis houses two transformers, the AC line filter and numerous fuses. A service outlet has been conveniently located on top of the chassis so that AC operated test equipment and lighting may be plugged into the game without the need for an additional wall socket.

Approximately 115 volts AC enters the power chassis via the line cord. The AC line filter blocks any noise that might enter via the line cord and a varistor protects against high voltage spikes. The 115 volts AC then leaves the power chassis and passes thru the power and safety switches. After the switches the 115 volts AC again enters the power chassis to supply the primary windings of the two transformers. Note the two voltage selection connectors that allow the power chassis to be operated at 105 volts, 115 volts or 125 volts AC.

The game transformer (MT-105A) has two secondary windings. The 30 volt winding is center tapped to yield two 15 volt lines and the 18 volt winding is center tapped to yield two 9 volt lines. To accurately measure the 9 volt and 15 volt lines use the 0 volt tap on each winding. Each of the 9 volt and 15 volt lines are fused. If fuses F3 and F4 on the 9 volt lines blow out frequently, use 5 amp. slo-blo fuses instead.

The MT-101A transformer isolates the monitor from the main AC line for safety purposes. This transformer also has a secondary winding of 12 volts. The 12 volt winding is fused and then sent to the power supply board along with the 9 volt and 15 volt lines from the game transformer.

The power supply was designed to provide three regulated outputs at +5, +12 and −5 volts DC and one unregulated output at approximately +16 volts DC. The Super Pac-Man system does not require the −5 volt circuitry or the battery back-up circuitry which might be provided on this board.

The combined Super Pac-Man logic boards (CPU and Video) draw approximately 3.25 amperes from the +5 volt output. The +12 volt output supplies the audio circuitry on the CPU board. The audio circuitry may draw between 90MA to 250MA depending on how loud the sound is set and whether or not sound is occurring. The unregulated +16 volt output is used across the coin door lites.

The two 15 volt AC taps from the game transformer are rectified by diodes D110 and D111 (A15F 3 amp.) and filtered by capacitor C104 (25,000μf 35 volts) to provide approximately +20 volts DC to the +12 volt regulator circuit.

The LM305 at position U5, transistors Q100 and Q104 and associated resistors and capacitors make up the +12 volt regulator circuit. Potentiometer VR102 can be adjusted to set the +12 volts to within ±.2 volt when measured at the logic boards.

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Pin number 8 of the LM305 at U5 senses the voltage drop across resistor R102. The voltage drop across a resistor is directly proportional to the current flowing thru the resistor. By sensing the voltage drop across resistor R102, the LM305 will detect excessive current drain and it will shut down the +12 volt regulator circuit before damage is done to either the power supply or logic boards.

When the +12 volt regulator circuit is functioning properly the base of Q104 will be approximately 17.5 to 20.5 volts and the base of Q100 will read approximately 12.5 to 13.5 volts when measured from the "common" line. Note that in the +12 volt regulator circuit the input of the LM305 (pin 3) and the collector of Q100 are both tied to the +20 volt DC line.

The "sense" line to the LM305 at U5 is connected to "common" via jumper JW2. Capacitor C114 (470μf 25 volts) offers additional filtering after the +12 volt regulator circuit.

The two 9 volt AC taps from the game transformer are rectified by diodes D106 and D107 (MR750 6 amp.) and filtered by capacitor C113 (40,000μf 16 volts). The result is approximately +12 volts DC which supplies the coin counter and the collector of the +5 volt pass transistor Q101.

In the +5 volt regulator circuit the input to the LM305 (pin 3) at position U2 is connected to the +20 volt DC line thru diode D103 and fuse F1. Pin 3 of the LM305 at U2 will read approximately 19.25 volts considering a voltage drop of .7 volt across diode D103. The LM305 senses the voltage drop across resistor R103 and will shut down the +5 volt regulator circuit if it detects a current drain exceeding 4 amperes. Potentiometer VR101 can be adjusted to set the +5 volts to within ±.2 volt when measured at the logic boards. Capacitor C102 (470μf 25 volts) offers additional filtering of the +5 volts DC. Resistor R134 (68 ohms 1/2 watt) is used as a dummy load and holds down the +5 volts when there is no external load. When the +5 volt regulator circuit is functioning properly the base of transistor Q102 will read approximately +16 volts and the base of Q101 will read +6.5 to 7 volts.

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NOTES

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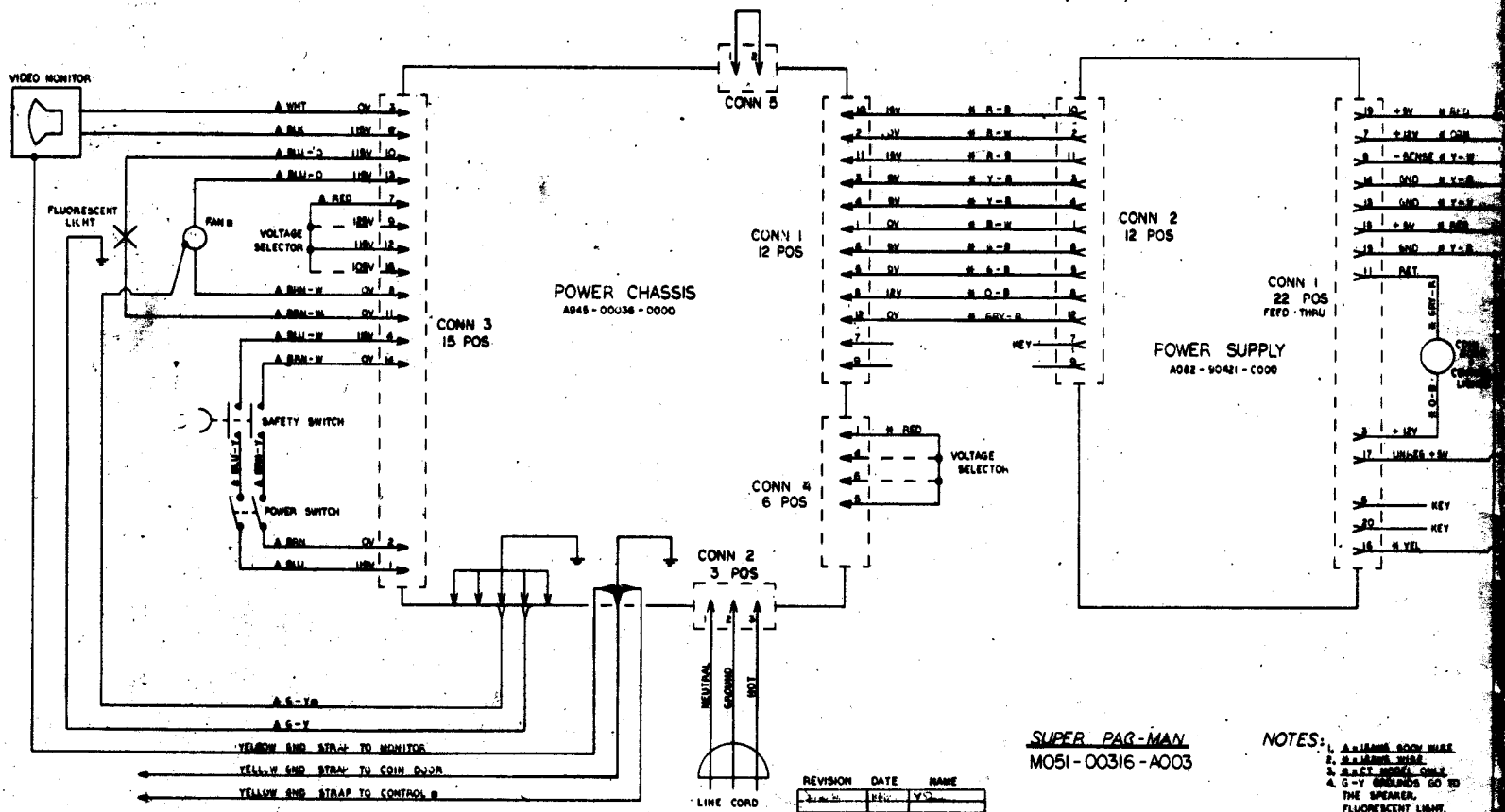
Schematics and Wiring Diagrams

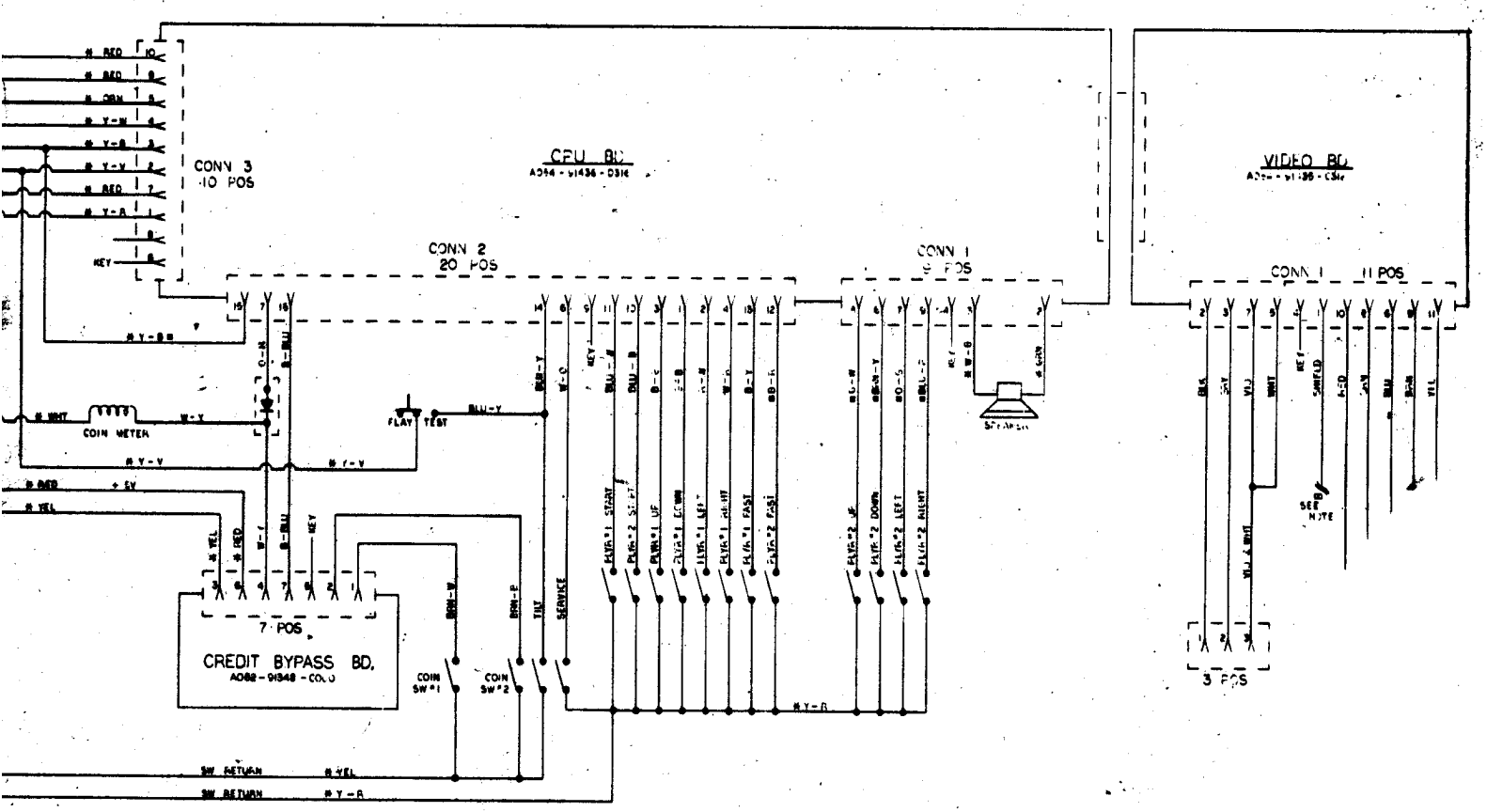


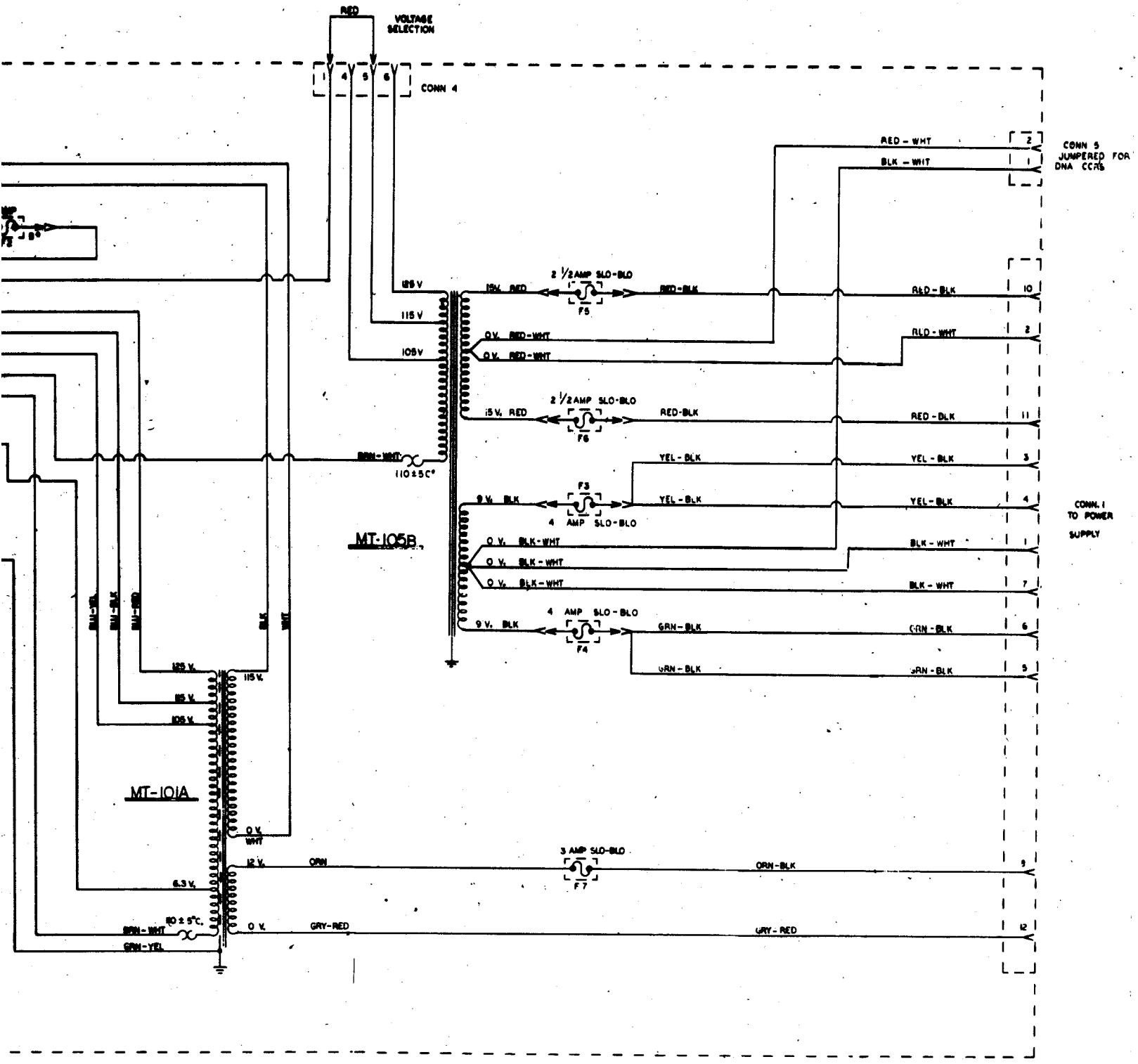
REVISION	DATE	NAME

SUPER PAC-MAN
M051-00316-A003

Bally / MIDWAY
10601 W BELMONT
FRANKLIN PARK, ILL 60131

NOTES:
1. A = 18AWG 600V WIRE
2. # = 18AWG WIRE
3. # = CT MODEL ONLY
4. G-Y GROUNDS GO TO THE SPEAKER, FLUORESCENT LIGHT, THE FAN ON THE CT
5. m = PINED AT LOGIC; CHE AT MONITOR JACK


CONN 3
10 POS
CPU BD
CONN 2
20 POS
CONN 1
VIDEO BD
CONN 1 11 POS
COIN METER
FLAY TEST
7 POS
CREDIT BYPASS BD.
COIN SW #1
COIN SW #2
SERVICE
SW RETURN
SW RETURN
3 POS
SEE NOTE



NOTES:
1. A* = WHEN USED
2. B* = BOTTOM TERMINAL
3. S* = SIDE TERMINAL
4. TS1-5 = TERMINAL BARRIER STRIP POSITIONS
5. ⏚ = CHASSIS EARTH GND.
6. (----) = ALTERNATE COLOR

POWER CHASSIS CT MODEL
70VA. 115V. 60Hz.
* M051-00945-A046

MIDWAY MFG CO.
10601 W. BELMONT AVE.
FRANKLIN PARK, ILL. 60131

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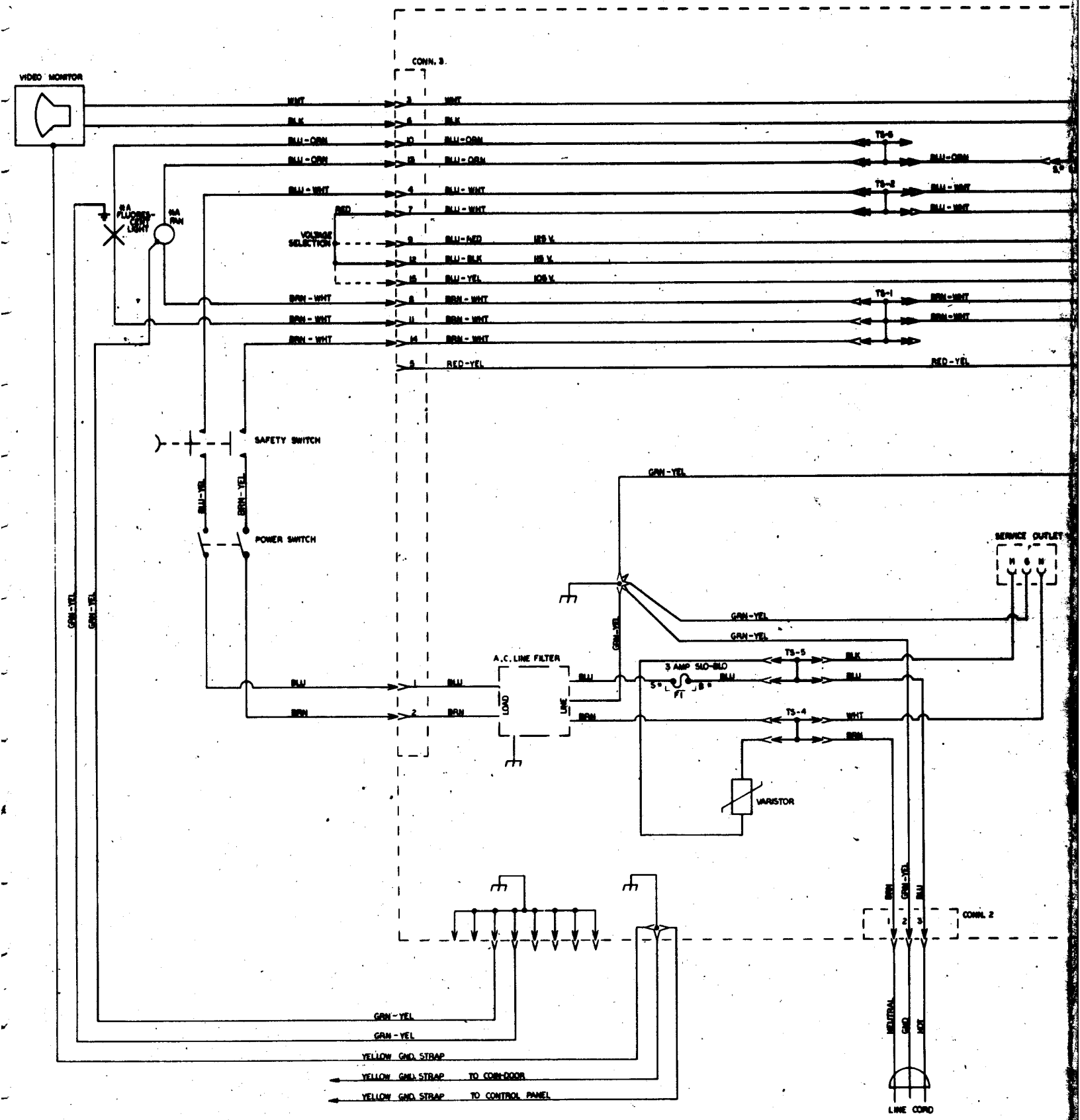
VIDEO MONITOR
CONN. 3
WHT
BLK
BLU-ORN
BLU-WHT
RED
VOLTAGE SELECTION
BLU-RED
BLU-BLK
BLU-YEL
BRN-WHT
RED-YEL
TS-6
TS-8
TS-1
8A FLUORES-CENT LIGHT
4A FAN
SAFETY SWITCH
POWER SWITCH
BLU-YEL
BRN-YEL
GRN-YEL
BLU
BRN
A.C. LINE FILTER
LOAD
LINE
3 AMP SLO-BLO
FT
TS-5
TS-4
WHT
VARISTOR
SERVICE OUTLET
N
G
N
CONN. 2
NEUTRAL
GND
HOT
LINE CORD
YELLOW GND. STRAP
YELLOW GND. STRAP TO CORE-DOOR
YELLOW GND. STRAP TO CONTROL PANEL

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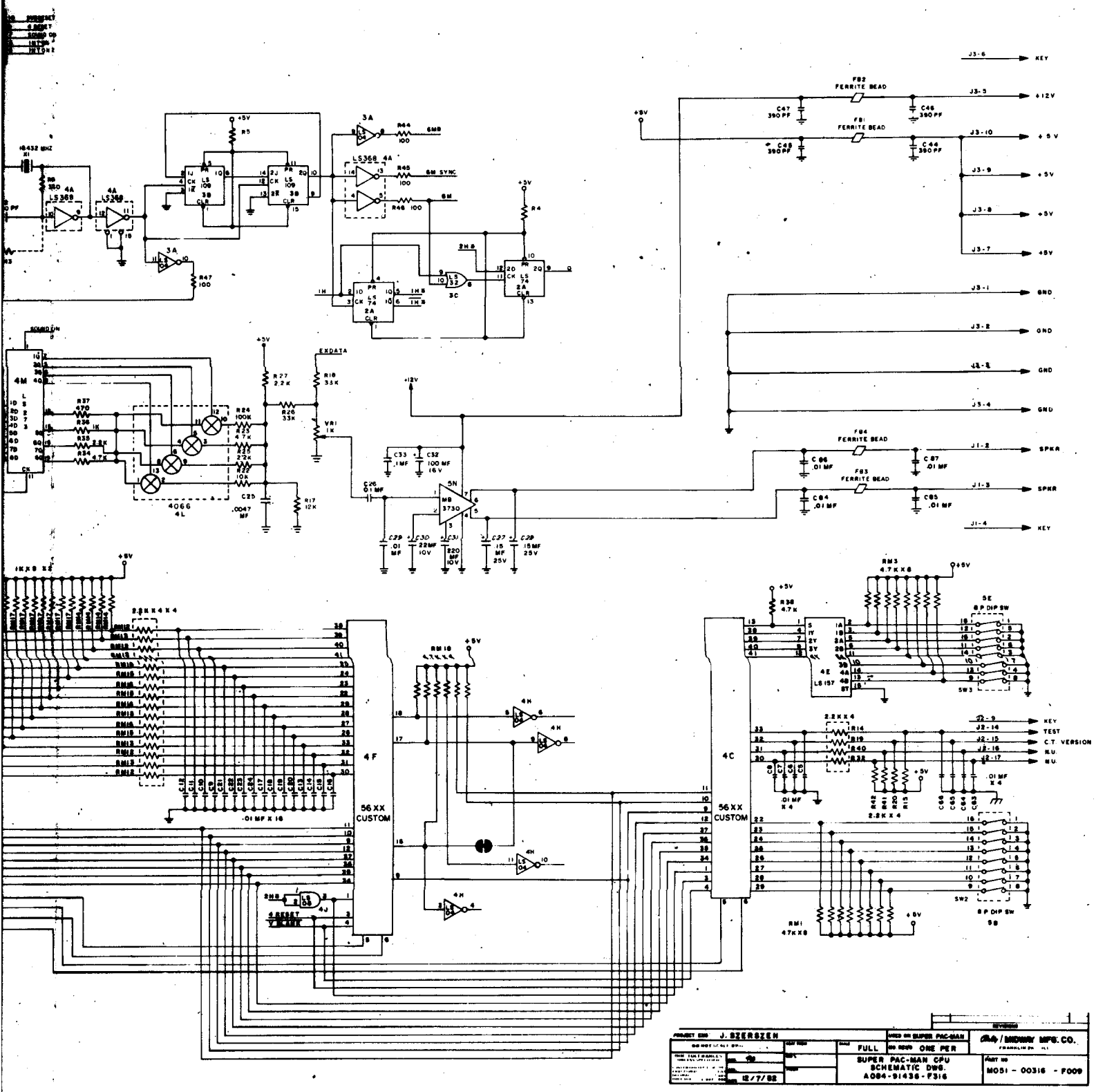

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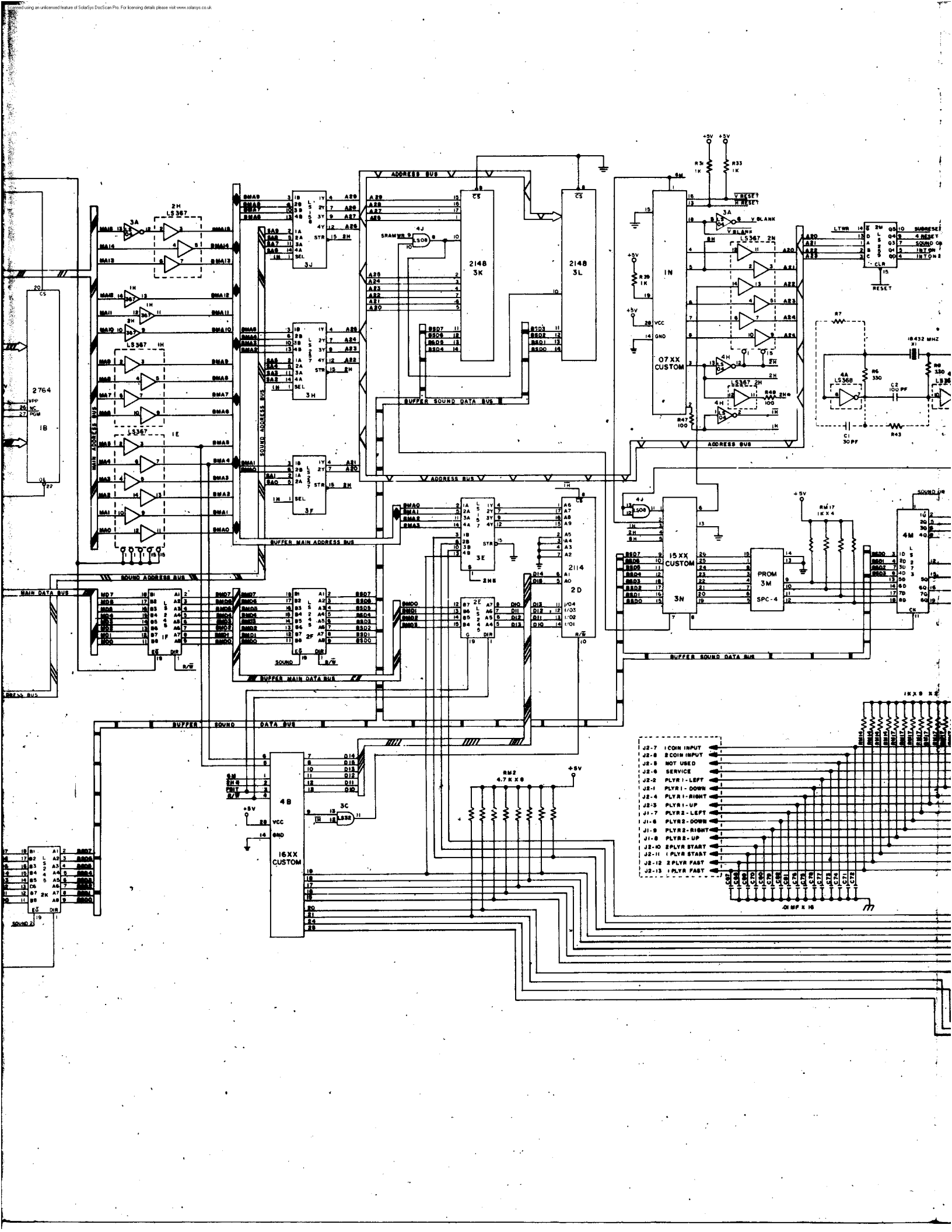

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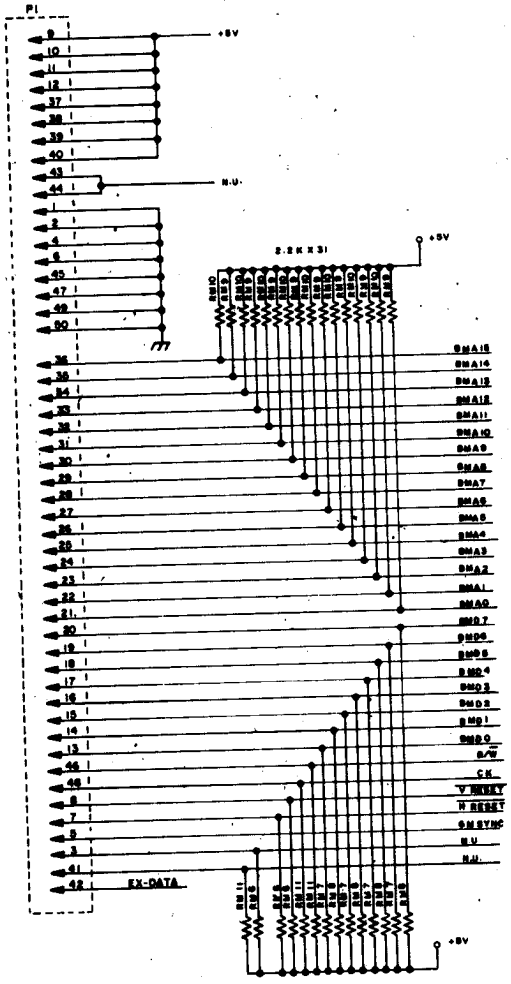

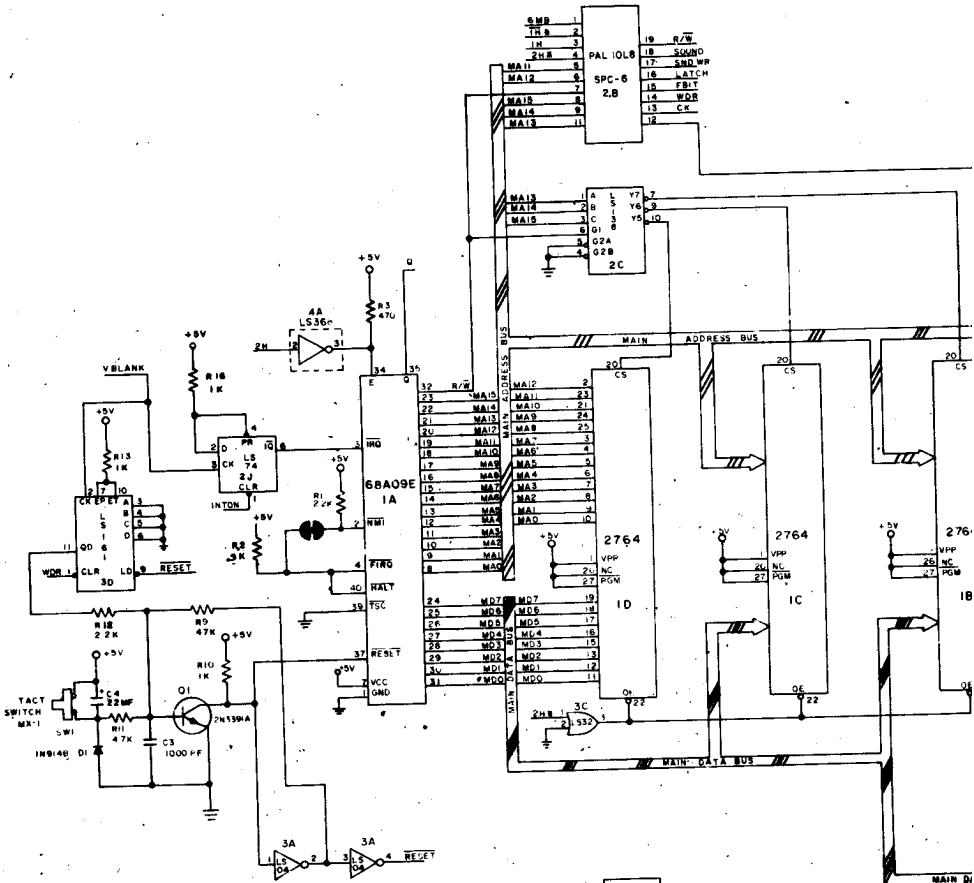

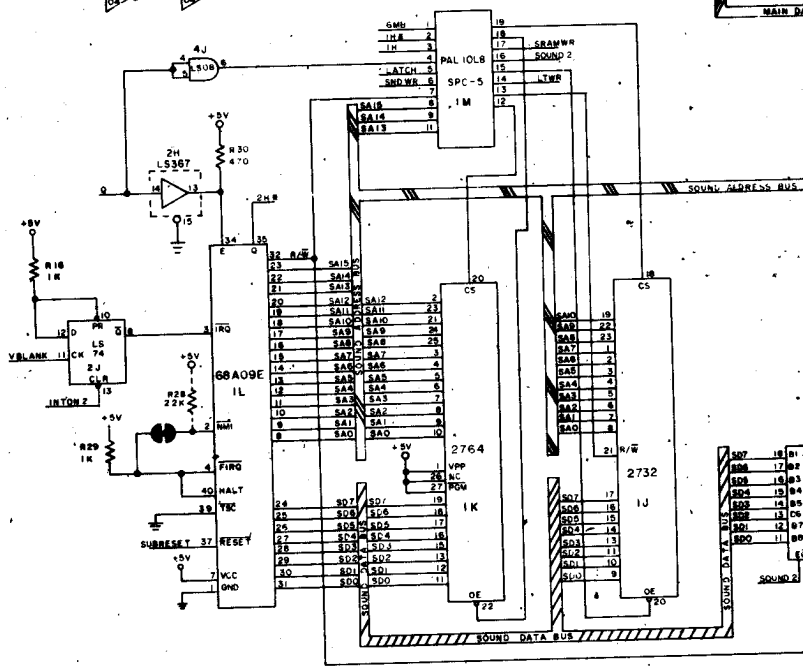

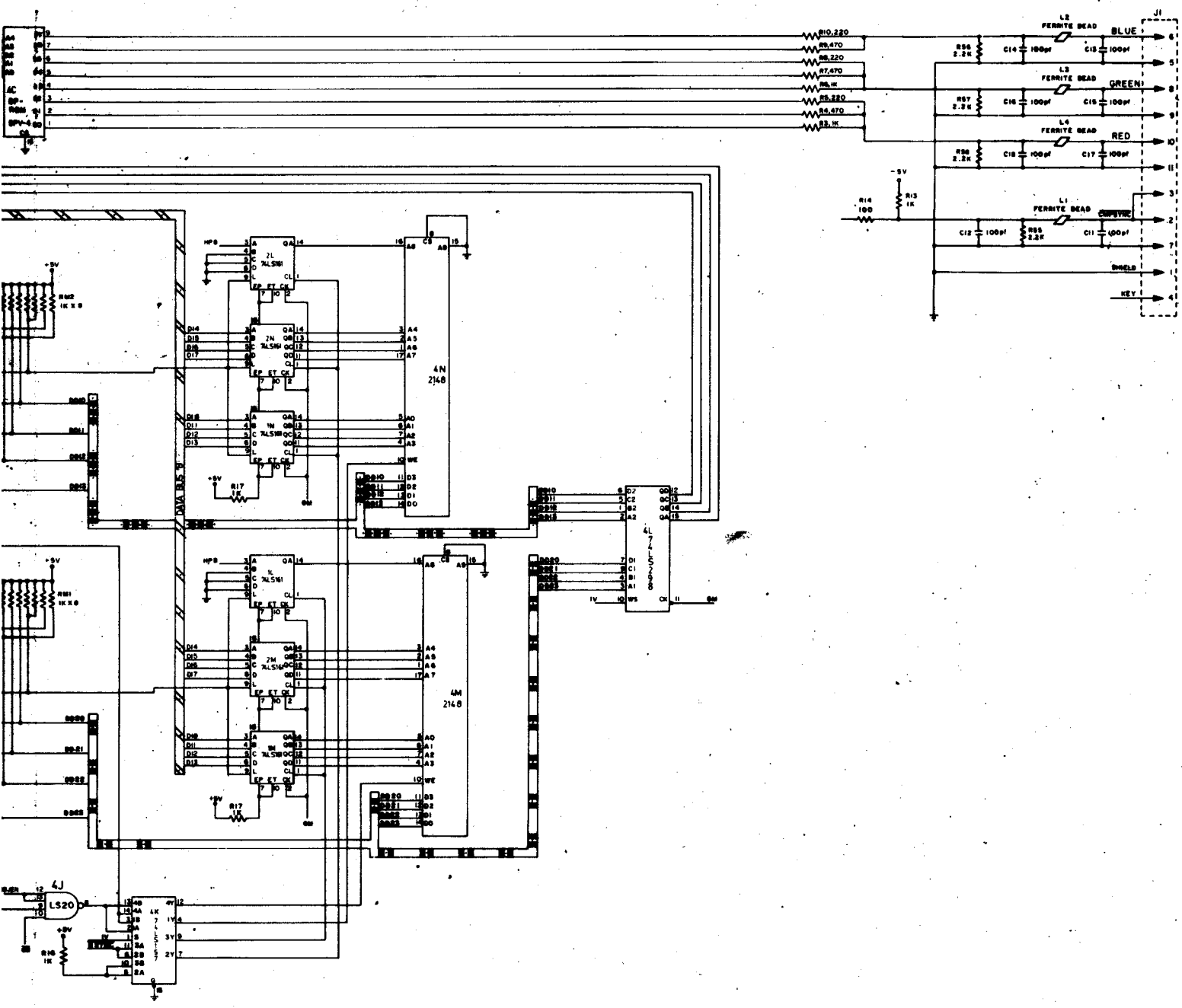

PROJECT ENG. J. SZERSZEN		USED ON SUPER PAC-MAN	MIDWAY MFG. CO. FRANKLIN PK. ILL.
DO NOT SCALE DRAWING		NO. REQD 1 PER.	
		SUPER PAC-MAN VIDEO BD. SCHEMATIC A084-91435-C316	PART NO. M051-00316-C007
	11/03/82		

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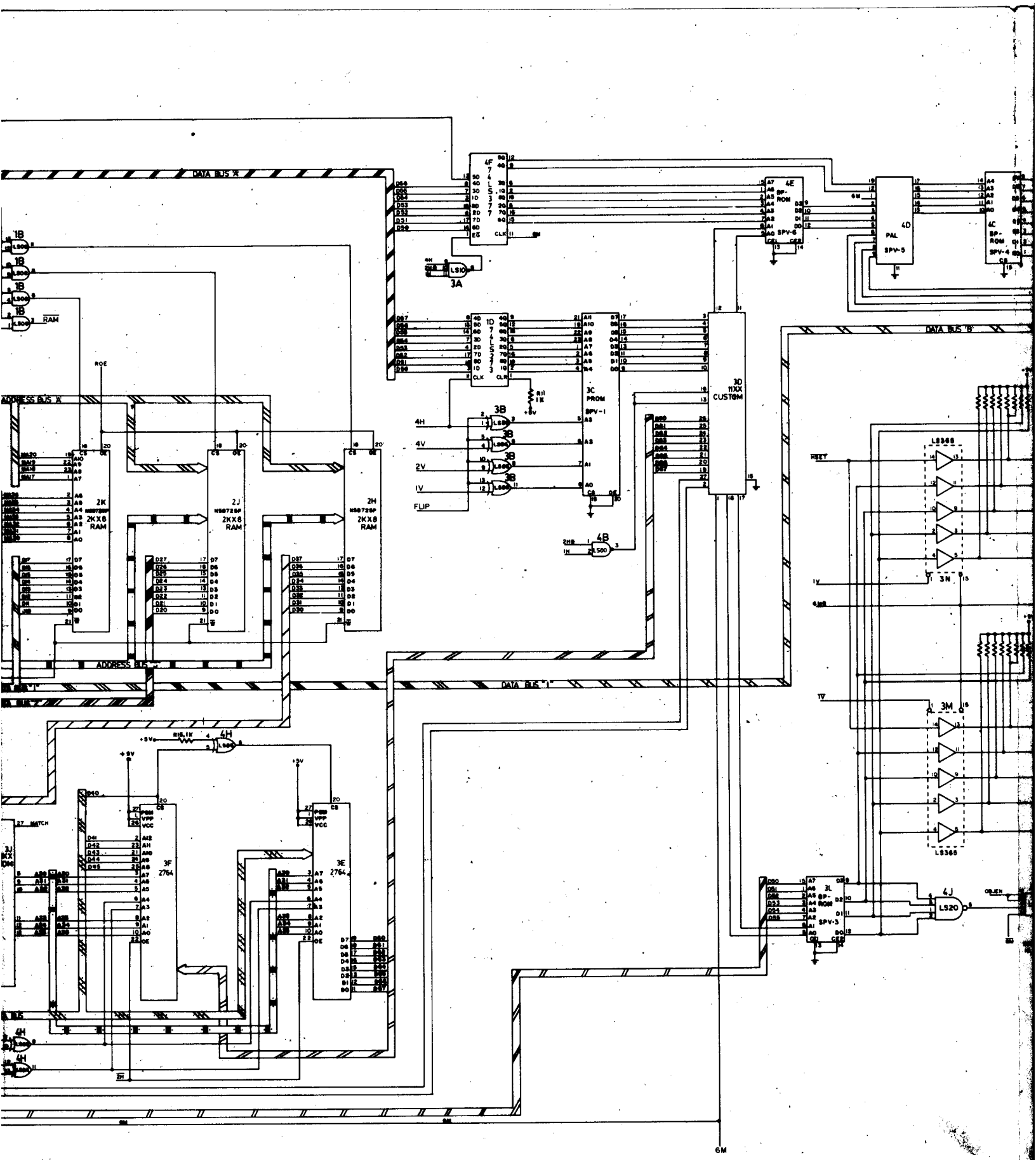
DATA BUS "A"
DATA BUS "B"
DATA BUS "1"
ADDRESS BUS "A"
ADDRESS BUS "B"
4F 74LS377
4E BP-ROM SPV-6
4D PAL SPV-5
4C BP-ROM SPV-4
3A LS10
1D 74LS373
3C PROM SPV-1
3D 11XX CUSTOM
3B
4B LS00
2K 2KX8 RAM
2J 2KX8 RAM
2H 2KX8 RAM
3F 2764
3E 2764
4H
3L BP-ROM SPV-3
4J LS20
3N LS365
3M LS365
4H
4V
2V
1V
FLIP
HSET
OBJEN
6M
RAM
ROE
MATCH

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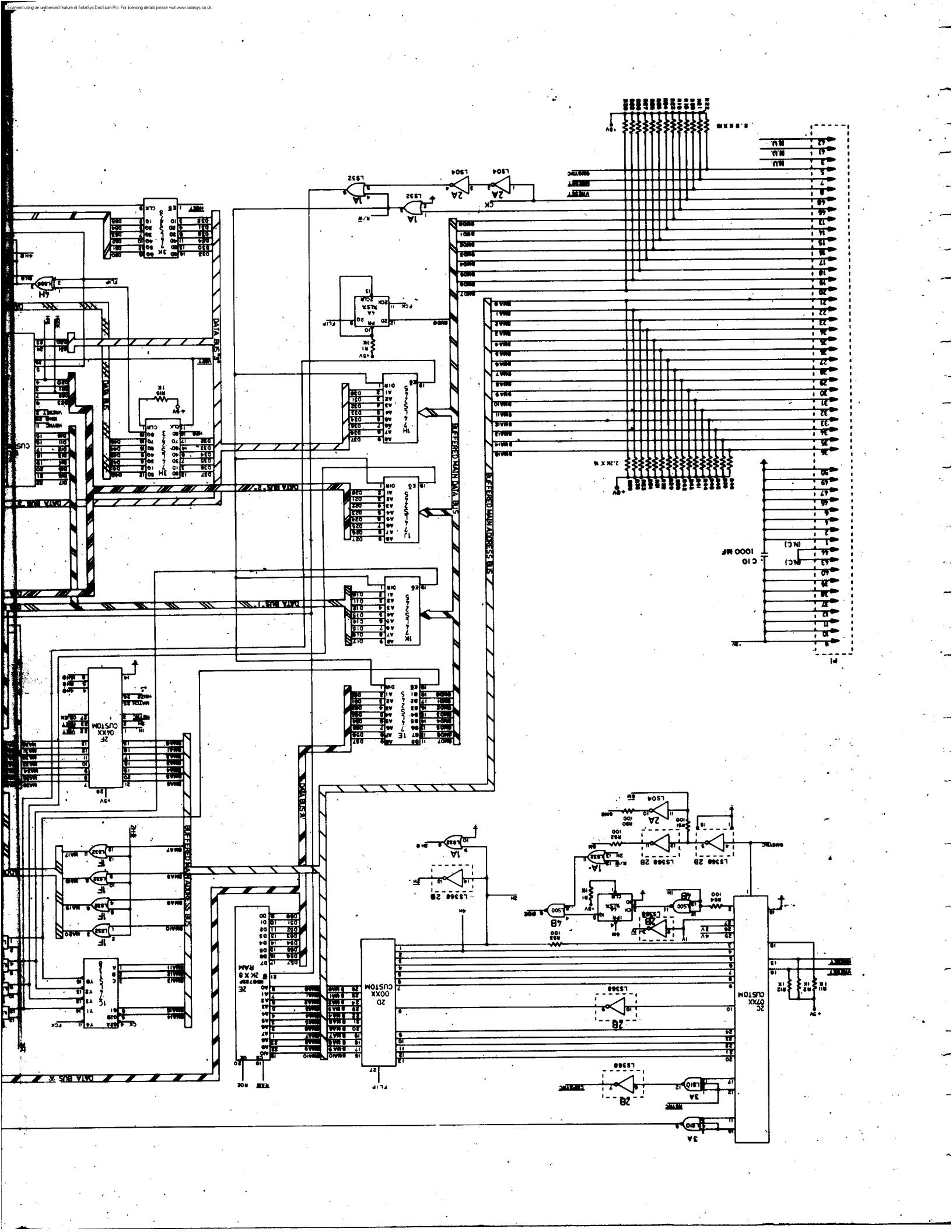

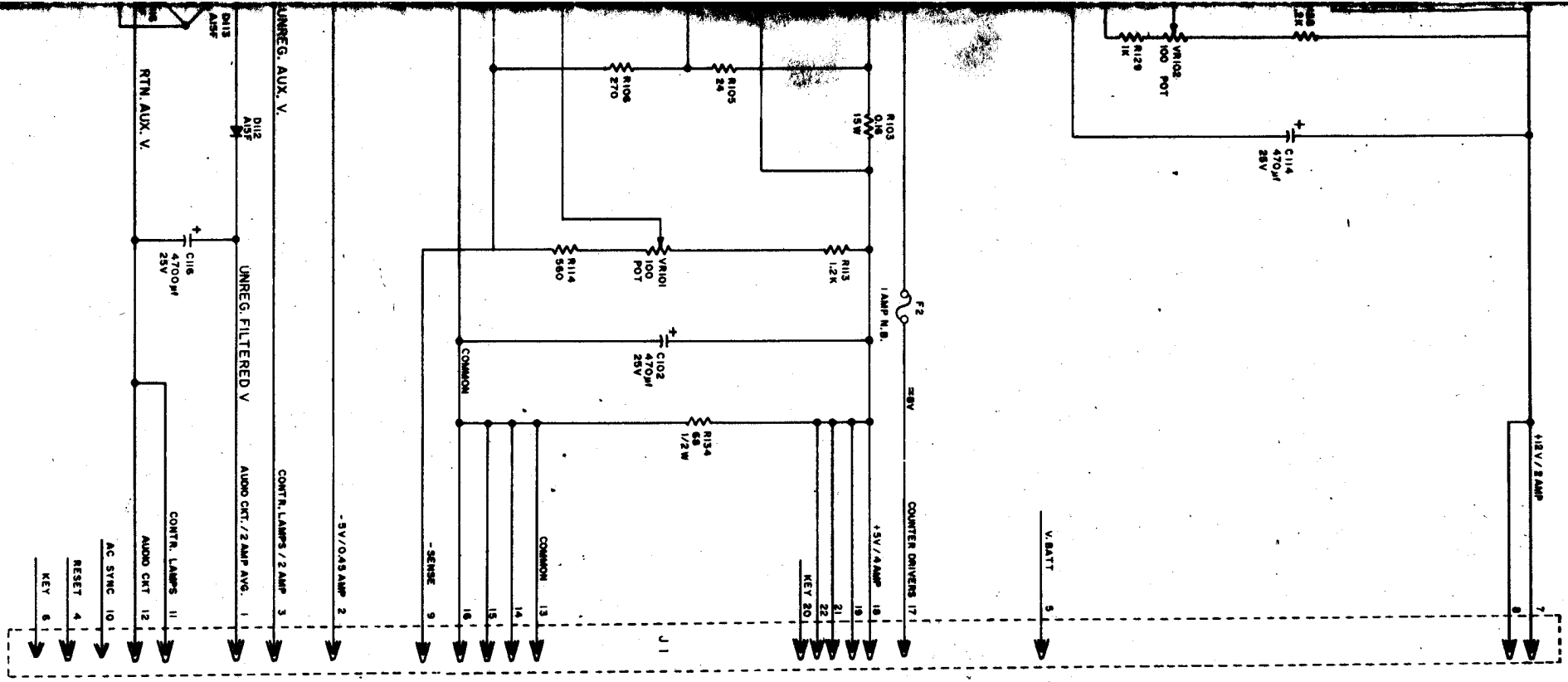

PROJECT ENG:		USED ON	Bally / MIDWAY MFG. CO. FRANKLIN PARK, ILL.
DO NOT SCALE DRAWING	DRAW TRACE	SCALE	NO. REQ'D
DRAWN RLW 12/02/82	DES.	MEDIUM PWR. SUPPLY 70 VA A082-90421-C000	PART NO M051-00945-A032

REVISIONS

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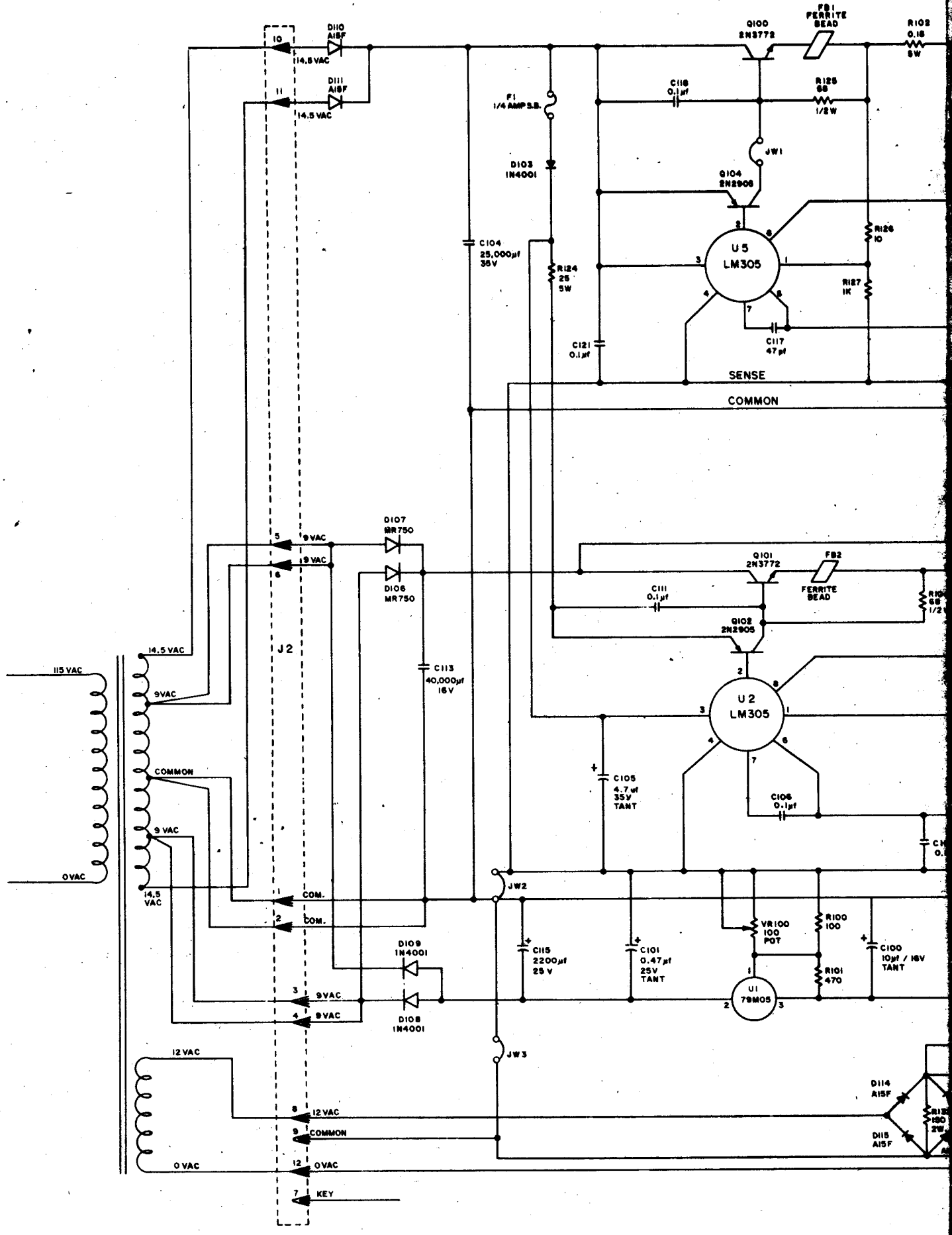
D110 A15F
14.5 VAC
D111 A15F
14.5 VAC
F1 1/4 AMP S.B.
D103 1N4001
Q100 2N3772
FB1 FERRITE BEAD
R102 0.1Ω 5W
C118 0.1μf
R125 68 1/2W
JW1
Q104 2N2906
C104 25,000μf 35V
R124 25 5W
U5 LM305
R126 10
R127 1K
C121 0.1μf
C117 47 pf
SENSE
COMMON
D107 MR750
D106 MR750
9 VAC
9 VAC
Q101 2N3772
FB2 FERRITE BEAD
C111 0.1μf
Q102 2N2905
J2
14.5 VAC
115 VAC
9VAC
COMMON
9 VAC
0VAC
14.5 VAC
C113 40,000μf 16V
U2 LM305
C105 4.7 μf 35V TANT
C106 0.1μf
JW2
COM.
COM.
D109 1N4001
D108 1N4001
C115 2200μf 25 V
C101 0.47μf 25V TANT
VR100 100 POT
R100 100
R101 470
U1 79M05
C100 10μf / 16V TANT
JW3
12 VAC
12 VAC
COMMON
0 VAC
0VAC
KEY
D114 A15F
D115 A15F

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November 29, 1982

SERVICE BULLETIN

GAME: SUPER PAC-MAN

SUBJECT: NEW COIN SWITCH CIRCUIT TO PREVENT STRINGING

CONDITION

1. When a coin hangs or the coin switch is operated manually with a long pulse the game will lock-up (credit will show AA).
2. The game will clear the lock-up condition by turning the power off and on.
3. The coin circuit will function normally with coins and will not cause a lock-up condition during normal play.

Andy Ducay
Service Manager

AD/dd

10601 W. Belmont Ave. • Franklin Park, Illinois 60131 • Telephone (312) 451-9200 • Telex: 72-1596

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November 29, 1982

SERVICE BULLETIN

GAME: SUPER PAC-MAN

SUBJECT: RACK TEST

1. Coin game.
2. Press 1 player button and start game.
3. When maze and characters appear, freeze game with Switch #8 in the ON position (Dip switch #2 at 5B).
4. Press speed button to advance racks from one stage to another.
5. Return Switch #8 to the OFF position to play game.

Andy Ducay
Service Manager

AD/dd

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December 14, 1982

SERVICE BULLETIN

GAMES: SUPER PAC-MAN

SUBJECT: POWER CHASSIS TWO 4 AMP. SLOW BLOW FUSES BLOWING

MODIFICATION

1. Replace the two 4 amp. slow blow fuses with 5 amp. slow blow fuses.

2. Check game electrically.

Andy Ducay
Service Manager

AD/dd

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February 2, 1983

A Glossary of Microprocessor Terms

MICROPROCESSOR — one or several microcircuits that perform the function of a computer's CPU. Sections of the circuit have arithmetic and comparative functions that perform computations and executive instructions.

CPU — central-processing unit. A computing system's "brain", whose arithmetic, control and logic elements direct functions and perform computations. The microprocessor section of a microcomputer is on one chip or several chips.

PROM — programmable read-only memory. User permanently sets binary on-off bits in each cell by selectively fusing or not fusing electrical links. Nonerasable. Used for low-volume applications.

EPROM — erasable, programmable, read-only memory. Can be erased by ultraviolet light bath, then reprogrammed. Frequently used during design and development to get programs debugged, then replaced by ROM for mass production.

ROM — read-only memory. The program, or binary on-off bit pattern, is set into ROM during manufacture, usually as part of the last metal layer put onto the chip. Nonerasable. Typical ROM's contain up to 16,000 bits of data to serve as the microprocessor's basic instructions.

RAM — random-access memory. Stores binary bits as electrical charges in transistor memory cells. Can be read or modified through the CPU. Stores input instructions and results. Erased when power is turned off.

LSI — large scale integration. Formation of hundreds or thousands of so-called gate circuits on semiconductor chips. Very large scale integration (VLS) involves microcircuits with the greatest component density.

MOS — metal-oxide semiconductor. A layered construction technique for integrated circuits that achieves high component densities. Variations in MOS chip structures create circuits with speed and low-power requirements, or other advantages (static will damage a MOS chip).

Andy Ducay
Service Manager

AD/dd

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MOTOROLA

MC6809E (1.0 MHz)
MC68A09E (1.5 MHz)
MC68B09E (2.0 MHz)

HMOS
(HIGH-DENSITY N-CHANNEL, SILICON-GATE)

8-BIT MICROPROCESSING UNIT

8-BIT MICROPROCESSING UNIT

The MC6809E is a revolutionary high performance 8-bit microprocessor which supports modern programming techniques such as position independence, reentrancy, and modular programming.

This third-generation addition to the M6800 family has major architectural improvements which include additional registers, instructions and addressing modes.

The basic instructions of any computer are greatly enhanced by the presence of powerful addressing modes. The MC6809E has the most complete set of addressing modes available on any 8-bit microprocessor today.

The MC6809E has hardware and software features which make it an ideal processor for higher level language execution or standard controller applications. External clock inputs are provided to allow synchronization with peripherals, systems or other MPUs.

M6800 COMPATIBLE

- Hardware — Interfaces with All M6800 Peripherals
- Software — Upward Source Code Compatible Instruction Set and Addressing Modes

ARCHITECTURAL FEATURES

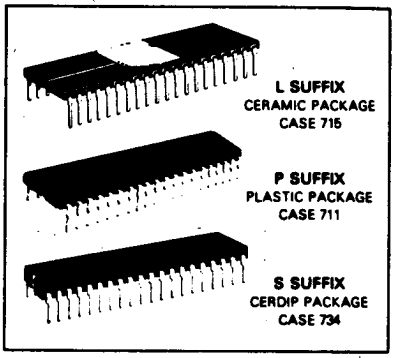
- Two 16-bit Index Registers
- Two 16-bit Indexable Stack Pointers
- Two 8-bit Accumulators can be Concatenated to Form One 16-Bit Accumulator
- Direct Page Register Allows Direct Addressing Throughout Memory

HARDWARE FEATURES

- External Clock Inputs, E and Q, Allow Synchronization
- TSC Input Controls Internal Bus Buffers
- LIC Indicates Opcode Fetch
- AVMA Allows Efficient Use of Common Resources in A Multiprocessor System
- BUSY is a Status Line for Multiprocessing
- Fast Interrupt Request Input Stacks Only Condition Code Register and Program Counter
- Interrupt Acknowledge Output Allows Vectoring By Devices
- SYNC Acknowledge Output Allows for Synchronization to External Event
- Single Bus-Cycle $\overline{\text{RESET}}$
- Single 5-Volt Supply Operation
- $\overline{\text{NMI}}$ Inhibited After $\overline{\text{RESET}}$ Until After First Load of Stack Pointer
- Early Address Valid Allows Use With Slower Memories
- Early Write-Data for Dynamic Memories

SOFTWARE FEATURES

- 10 Addressing Modes
  - M6800 Upward Compatible Addressing Modes
  - Direct Addressing Anywhere in Memory Map
  - Long Relative Branches
  - Program Counter Relative
  - True Indirect Addressing
  - Expanded Indexed Addressing:
    - 0, 5, 8, or 16-bit Constant Offsets
    - 8, or 16-bit Accumulator Offsets
    - Auto-Increment/Decrement by 1 or 2
- Improved Stack Manipulation
- 1464 Instructions with Unique Addressing Modes
- 8 × 8 Unsigned Multiply
- 16-bit Arithmetic
- Transfer/Exchange All Registers
- Push/Pull Any Registers or Any Set of Registers
- Load Effective Address

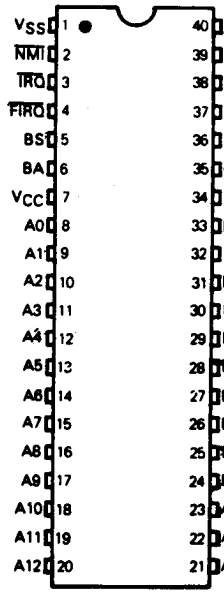


L SUFFIX
CERAMIC PACKAGE
CASE 715

P SUFFIX
PLASTIC PACKAGE
CASE 711

S SUFFIX
CERDIP PACKAGE
CASE 734

FIGURE 1 — PIN ASSIGNMENT



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SUPER PAC-MAN CPU BOARD
(P.C. A084-91436-C316)

Chip Number	Function
74LS04	Hex Inverters
74LS08	Quad 2 Input AND
74LS32	Quad 2 Input OR
74LS74	Dual D Type Flip-Flop
74109	Dual JK Type Flip-Flop
74LS138	3 to 8 Line Decoder/Multiplexer
74LS157	Quad 2 to 1 Line Multiplexer
74LS158	Quad 2 to 1 Line Multiplexer — Inverted Outputs
74LS161	4 Bit Binary Counter
74LS245	Octal Bus Transceivers
74LS257	Quad 2 to 1 Line Multiplexer — Tri State
74LS259	8 Bit Addressable Latches
74LS273	Octal D Type Flip-Flop
74LS367	Hex Bus Drivers
74LS368	Hex Bus Drivers — Inverting
MC68A09	CPU

Chip Number	Function
2764	8K x 8 EPROM
2732	4K x 8 EPROM
AM9114	1K x 4 RAM
MBM2148	1K x 4 RAM
2114	1K x 4 RAM
SP1-1	PAL
SP1-2	PAL
SP1-3	256 x 4 PROM M7052
18.4320	Crystal
MC14066	Quad Bilateral Switches
MB3730	Audio Amplifier
07XX	Custom Horizontal & Vertical Sync Generator
15XX	Custom Address Generator
16XX	Custom Bus Controller
56XX	Custom I/O Ports

SUPER PAC-MAN VIDEO BOARD
(P.C. A084-91435-C316)

Chip Number	Function
74LS00	Quad 2 Input NAND
74LS04	Hex Inverters
74LS08	Quad 2 Input AND
74LS10	Triple 3 Input NAND
74LS20	Dual 4 Input NAND
74LS32	Quad 2 Input OR
74LS74	Dual D Type Flip-Flop
74LS86	Quad 2 Input XOR
74LS138	3 to 8 Line Decoder/Multiplexer
74LS157	Quad 2 to 1 Line Multiplexer
74LS161	4 Bit Binary Counter
74LS245	Octal Bus Transceivers
74LS273	Octal D Type Flip-Flop
74LS298	Quad 2 Input Multiplexer (With Storage)
74LS365	Hex Bus Drivers
74LS368	Hex Bus Drivers — Inverted Outputs

Chip Number	Function
74LS377	Octal D Type Flip-Flop
74LS378	Hex D Type Flip-Flop
2764	8K x 8 EPROM
2732	4K x 8 EPROM
2148	1K x 4 RAM
M58725	2K x 8 RAM
00XX	Custom Address Generator
04XX	Custom Address Buffer
07XX	Custom Horizontal & Vertical Sync Generators
11XX	Custom Bit Shifter
12XX	Custom Address Generator
SP1-7	PAL
3160-15AXL-CXPD	256 x 4 PROM
3160-15AXL-BXPD	256 x 4 PROM
3160-03AAC-AXPD	32 x 8 PROM

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